Highly Rectifying Silicon Schottky Contacts Using Energetically Deposited Graphitic Carbon

A thesis submitted in fulfilment of the requirements for the degree of

Doctor of Philosophy

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Declaration

I certify that except where due acknowledgement has been made, the work is that of the author alone; the work has not been submitted previously, in whole or in part, to qualify for any other academic award; the content of the thesis is the result of work which has been carried out since the official commencement date of the approved research program; any editorial work, paid or unpaid, carried out by a third party is acknowledged; and, ethics procedures and guidelines have been followed.

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Mohammad Saleh N Alnassar

December 2017

To

My Mother Intisar

Acknowledgments

The accomplishment of this work would never be possible without the financial, administrative, academic, and emotional support from many institutions and individuals.

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ABSTRACT

The formation of high quality Schottky diodes (i.e. high rectification ratio, low saturation current, low series resistance, and ideality factor close to 1) by Filtered Cathodic Vacuum Arc deposition of carbon (FCVA C) onto p-type silicon substrates has been demonstrated in this thesis. Electrical measurement results clearly indicate that the choice of FCVA's deposition parameters (i.e. energy and temperature) have an influence on the quality of the Schottky junction. Moreover, these measurements have assisted in identifying both the effect of the varying microstructure of graphitic carbon films (sp^2/sp^3 ratio) caused by different deposition parameters and the presence of a thin, resistive interfacial layer between carbon and p-Si. Technology Computer Aided Design (TCAD) simulations based on a Metal-Insulator-Semiconductor (M-I-S) and on a Metal-Resistor-Semiconductor (M-R-S) diode structures were constructed to fit the experimental data. The M-I-S diode structure is a 2-D model where the interfacial layer was considered as an insulator. This model estimates the 'metal' work function and the thickness of the interfacial layer to approximate the experimental *I-V* results. The alternative M-R-S diode structure utilised 2-D and 3-D models to simulate the electrical behaviour of carbon/p-Si diodes. The primary feature in the M-R-S 2-D and 3-D models is the definition of a resistive interface (representing experimentally observed carbon/Si mixed interfacial layer) between the graphitic carbon thin film and Si. In addition to metal work function determination, *Schottky barrier lowering* can be incorporated in the M-R-S model to include image force effects reported in literature. Both models achieved excellent agreement with the measurement results in the forward *I-V* region. For the M-R-S model, the agreement with the

measurement results in the reverse *I-V* region has improved significantly compared to simulation using the M-I-S model. The M-R-S model provided information that could not be obtained from measurements and suggested a path to improved devices.

1 Introduction

1.1 Background

The earliest investigation on Metal-Semiconductor (MS) interfaces was published in 1874 by K. F. Braun [1]. He noted the current rectifying behaviour of various metal sulphides such as Galena when point-contacted with the tip of a fine metal wire. About three decades later, the cat's whisker (sometimes called crystal) detector, which was based on the point-contact structures originally described by Braun, started to gain fame after being commercialised by G. W. Pickard [2]. Although Braun's pioneering observations were not appreciated until 1909, when he shared a Noble Prize in Physics with Marconi, they contributed significantly to the development of several practical applications such as the radio, wireless telegraphy and World War II radar equipment [3]. Since then, MS interfaces have been extensively studied and developed.

In 1938, the Schottky Barrier Height (SBH) concept was introduced to explain the rectifying and nonlinear behaviour of MS junctions. By 1940, W. Schottky [4] and N. F. Mott [5], on separate occasions, established what is known today as the Schottky-Mott rule. Later, such junctions became known as Schottky junctions to honour Schottky for his contribution in understanding their physics.

Ideally, MS contacts can be classified either as Schottky (rectifying behaviour) or ohmic (obey Ohm's Law) depending on the interface characteristics. However, practical contacts are neither perfectly Schottky nor perfectly ohmic. Figure 1.1 shows

the dissimilarity in Current-Voltage (*I-V*) characteristics between an ohmic and a Schottky contact.

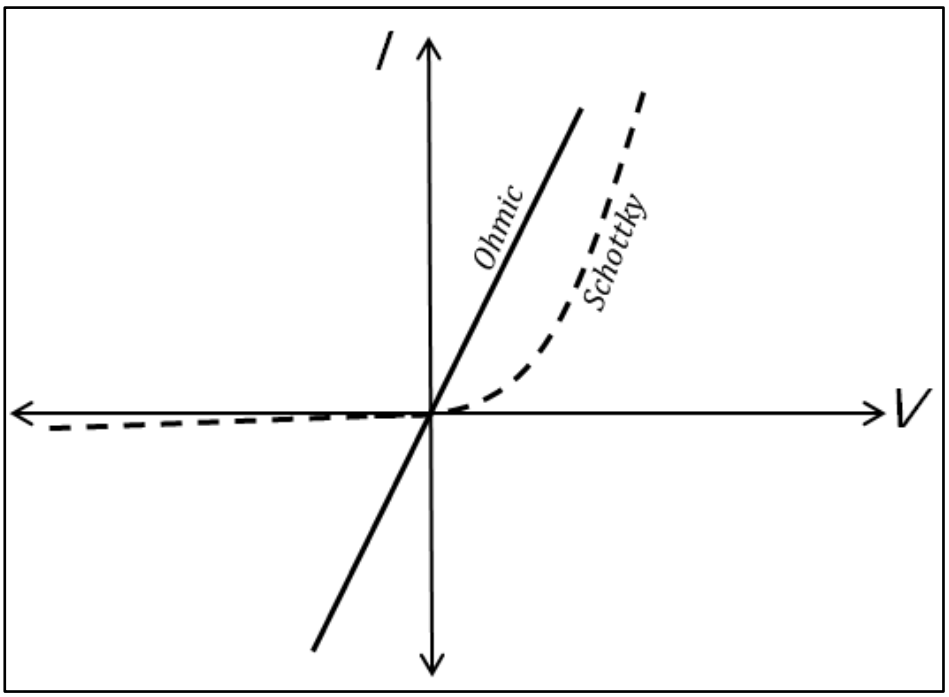

Figure 1.1: Typical *I-V* characteristics observed in an ohmic and a Schottky contact.

1.2 Motivation

Metal-semiconductor (MS) interfaces play a vital role in virtually all semiconductor devices. They are mainly utilised as contacts for semiconductor devices, e.g., Metal Oxide Field Effect Transistors (MOSFETs), Metal Semiconductor Field Effect Transistors (MESFETs), High Electron Mobility Transistors (HEMTs), Radio Frequency (RF) devices, Sensors/Detectors and solar cells. The properties of MS interfaces have a dominant influence on the stability, reliability, and performance of semiconductor devices [6]. In addition, forming and characterising different Schottky diodes is an excellent process for identifying promising novel materials for

the semiconductor industry due to their simple, low-temperature (for the Schottky junction at least), and low-cost processing requirements. The ability to understand the physical and chemical properties of a Schottky junction will greatly simplify the characterisation, and hence aid in the development of new semiconductor material systems.

Due to its ability to form hybridised bonds, carbon exists in a number of interesting structural forms in nature. The carbon atom has 4 valence electrons having either sp (as in amorphous carbon), sp^2 (as in graphite) or sp^3 (as in diamond) hybridised orbitals, thus contributing to the formation of three different hybridised bonds with neighbouring carbon atoms. Figure 1.2 shows three different forms (known as allotropes) of carbon.

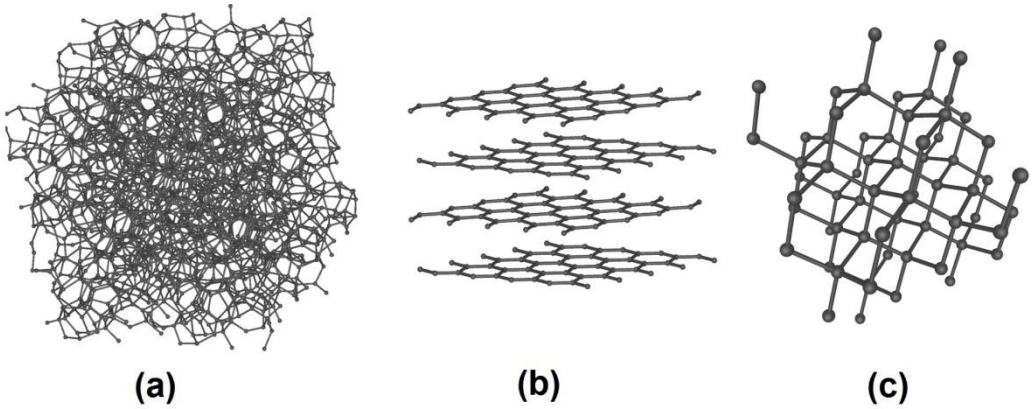

Figure 1.2: Different forms of carbon, (a) amorphous carbon, (b) graphite, and (c) diamond (redrawn after ref. [7]).

Since the renowned demonstration of graphene exfoliation from graphite in 2004 [8], tremendous work has been devoted to integrate both 2D graphene and its 3D sibling, graphite, as metal (semimetal) contact into various semiconductor devices.

Nevertheless, exploiting the unique properties of these carbonaceous materials in large scale integrated circuits remains elusive.

Graphene [9-11] and graphitic carbon [12, 13] thin films have attracted a great deal of interest in recent years. Studies demonstrated that they form high quality Schottky diodes (i.e. High rectification ratios, low saturation current, and ideality factors close to unity) [11]. The carbon thin films in these diodes were formed by the mechanical exfoliation method [9, 12] and Chemical Vapour Deposition (CVD) [10, 11, 13]. An important requirement in carbon/Si Schottky diodes has been the presence of a sufficient amount of the conductive graphite-like sp^2 phase. The ratio of the sp^2 phase to the diamond-like sp^3 phase in the aforementioned deposition methods was often difficult to control. Energetic deposition methods such as cathodic arc deposition have enabled more precise control over the sp^2/sp^3 ratio in the as-deposited film [14-16].

At the School of Science at RMIT University, graphitic carbon can be energetically deposited onto different types of substrates using a Filtered Cathodic Vacuum Arc (FCVA) deposition system [14-16]. The ability to tune the material's optical, electrical, and structural properties to various device applications such as Schottky diodes is a feature of carbon-based thin films formed using this technique. Therefore, demonstration of high quality carbon/Si Schottky diodes fabricated using the FCVA system is a principal objective in this thesis.

In conjunction with experimental fabrication and testing, Technology Computer Aided Design (TCAD) simulation tools are becoming more and more

strategic and useful not only in predicting the performance of future generation devices but also as an efficient method to experiment, analyse, and thus determine the viability of novel materials and concepts [17]. Consequently, the formidable cost and timeframe challenges to improve a novel technology can be confronted by providing more specific guidelines with regard to materials and structures in performance optimisation. According to the International Technology Roadmap for Semiconductors (ITRS), TCAD can lower technology development costs up to 40% by reducing the number of experimental lots and shortening development time [18]. Simulation has the advantage of being very economic research tool. This is a crucial advantage for research students in university settings. In addition, there are various phenomena that cannot be measured experimentally (e.g. distribution of electrostatic potentials and current densities within the real device structure); simulations offer unique insight and hence enhance the understanding of semiconductor device physics by allowing the observation of such entities.

1.3 Research Description

In this thesis, the electrical characteristics of carbon/ p-Si interfaces are investigated experimentally and modelled numerically. Carbon thin films (with varying microstructures) were energetically deposited onto p-type Si substrates using a Filtered Cathodic Vacuum Arc (FCVA) System to form Schottky barrier diodes. Results of current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) measurements to evaluate the junction quality of the fabricated samples are presented. In addition, Pt/p-Si Schottky barrier diodes were fabricated on identical p-Si substrates and characterised in the same manner to allow for direct comparison. Hall Effect measurements were performed on the Si substrate in order to obtain an accurate value

of the carrier density. Numerical modelling for all samples was accomplished using state-of-the-art Technology Computer Aided Design (TCAD) tools.

1.4 Research Outcomes Specification

In this investigation, successful operation of high quality carbon/p-Si Schottky diodes has been demonstrated. The performance of these diodes was measured and the results indicate that FCVA carbon thin films form low cost yet higher quality (particularly in regard to rectification ratio) Schottky diodes to p-Si compared to conventional metals. In addition, TCAD was successfully utilised to explain the measured characteristics of the fabricated samples.

1.5 Thesis Organisation

This thesis has been structured into chapters, sections, and subsections in order to enable the reader to access specific entities of this work. This thesis primarily reports and discusses the fabrication, electrical characterisation, and TCAD simulation (in 2D and 3D) of carbon/p-Si Schottky diodes.

Chapter 2 lays the foundation of this thesis by briefly reviewing ideal Metal-semiconductor theory (i.e. Schottky-Mott model). This includes a discussion about electrical characterisation of Schottky diodes, particularly how the Shcottky Barrier Height (SBH) and other performance figures are measured in practice. Next, an introduction to numerical simulation of semiconductor devices is presented followed by an overview for each tool used in Sentaurus TCAD to simulate the electrical behaviour of the fabricated diodes. Most importantly, it reports key device-physics

equations and provides the details about the carrier transport model adopted in in the Metal-Resistor-Semiconductor (M-R-S) modelling approach presented in chapter 4. The final section in this chapter provides a review on C/Si devices reported in literature.

Chapter 3 details all experimental conditions and parameters used in the fabrication and characterisation of C/p-Si and Pt/p-Si Schottky diodes.

Chapter 4 presents the Metal-Resistor-Semiconductor M-R-S based structure as a modelling approach to simulate the *I-V* characteristics of the fabricated C/p-Si diodes. This includes the details of the geometries in 2D and 3D mode. Most importantly, it describes how this TCAD approach captures the observed resistive effects of both the C-Si interfacial layer and the varying microstructure of the FCVA carbon thin films.

Chapter 5 begins by reporting and discussing the electrical characterisation results of the fabricated samples. It then presents modelling results of 2-D Metal-Insulator-Semiconductor (M-I-S) diode structure to approximate the experimental results. Finally, the reliability of the M-R-S modelling approach in interpreting the interfacial effects observed in the fabricated samples is demonstrated by showing the effect of varying key parameters in the model.

Chapter 6 concludes this thesis by listing the achieved research outcomes and proposing possible avenues for future work.

1.6 Publication List

M. S. N. Alnassar, P. W. Leech, G. K. Reeves, A. S. Holland, D. W. M. Lau, D. G. McCulloch, H. N. Tran, and J.G. Partridge, "Graphitic Schottky Contacts to Si formed by Energetic Deposition," *Materials Research Society (MRS) Online Proc.*, vol. 1786, pp. 51-56, 2015.

M. S. N. Alnassar, S. Luong, H. N. Tran, J.G. Partridge, and A. S. Holland, "Simulation of graphitic contacts to p-type Si using a Metal-Resistor-Semiconductor (M-R-S) model implemented in TCAD," *International Journal of Numerical Modelling: Electronic Networks Devices and Fields,* 2017, DOI: 10.002/jnm.2302

M. S. N. Alnassar, P. W. Leech, G. K. Reeves, A. S. Holland, D. W. M. Lau, D. G. McCulloch, H. N. Tran, and J.G. Partridge, "High Rectification Ratio Silicon Schottky Diodes using Graphitic Carbon," submitted to Materials Letters.

Stanley Luong, **Mohammad Saleh N. Alnassar**, Pan Yue, and Anthony S. Holland, "Optimisation of Schottky electrode geometry," *Proc. of SPIE Micro+Nano Materials, Devices, and Systems*, Vol. 9668, 96685P-1, Sydney, Australia, 2015.

H.N. Tran, T.A. Bui, G.K. Reeves, P.W. Leech, J.G. Partridge, **M.S.N. Alnassar**, and A.S. Holland, "Optimising the Rectification Ratio of Schottky Diodes in n-SiC and n-Si by TCAD," *MRS Advances*, vol. 1, pp. 3655–3660, 2016.

Stanley Luong, **Mohammad Alnassar**, Cao Dao, Deming Zhu, James Wang, and Anthony Holland, "Electrical characterisation of metal contacts to 4H-SiC enhanced

by pre-metalisation surface treatment," *Proc. of the International Symposium on Semiconductor Manufacturing (ISSM)*, Tokyo, Japan, 2016.

Stanley Luong, Yue Pan, **Mohammad S. Alnassar**, and Anthony Holland, "Improvement of Schottky power diode performance by electrode geometry and surround trenching of Schottky contact," *Proc. of the IEEE Region 10 Conference (TENCON)*, pp.2403-2405, Singapore, 2016.

Anthony S. Holland, Yue Pan, **Mohammad Saleh N. Alnassar**, and Stanley Luong, "CIRCULAR TEST STRUCTURES FOR DETERMINING THE SPECIFIC CONTACT RESISTANCE OF OHMIC CONTACTS," *Facta Universitatis, Series: Electronics and Energetics*, vol. 30, pp. 313-326, 2017.

Stanley Luong, Fahid Algahtani, **Mohammad Saleh N. Alnassar**, Pan Yue, and Anthony S. Holland, "Circular Cross Kelvin Resistor test structure for low specific contact resistivity," *Proc.of the IEEE SouthEastCON*, Charlotte, USA, 2017.

Fahid Algahtani, Stanley Luong, Yue Pan, **Mohammad S. Alnassar**, and Anthony Holland, "A comparison of the Tri-Layer Transmission Line Model and a Finite Element Model for Ohmic Contact Analysis," *Proc. Of the 30th International Conference on Microelectronics (MIEL)*, Niš, Serbia, 2017 (Accepted).

2 Background

This chapter begins with a brief review of Metal-semiconductor contact theory. Also, it highlights some of the observed deviations from ideal MS theory and presents methods to measure the SBH and other performance figures. The chapter then lays the foundation for chapter 4 with an introduction to numerical modelling of semiconductor devices. The final section in this chapter provides a review on C/Si devices reported in literature.

2.1 MS Contacts

2.1.1 Introduction

MS contacts play a vital role in virtually all semiconductor devices; therefore, it is essential to understand the physical and chemical properties of these components. MS interfaces have been extensively studied and developed since the early 1930s. During this time, improvements were made in the performance of various semiconductor devices including the Schottky diode. The properties of MS interfaces are the dominant influence on the stability, reliability, and performance of the semiconductor devices.

MS junctions are characterised by their Schottky Barrier Height (SBH). Interfacial atomic rearrangement, inter-diffusion, and inter-metallic compound formation resulting from chemical equilibrium have a serious effect on the electronic equilibrium responsible for Schottky barrier formation [19]. Therefore, the SBH is a function of the atomic structure and atomic inhomogeneities along the interface which are caused by a mixture of different phases, grain boundaries, defects, etc. [20, 21]. The subsequent sections in this chapter present a brief review of some theoretical aspects related to MS contacts with extra focus on Schottky contacts. Most importantly, practical deviations from the ideal theory will be discussed. Also, barrier

height measurement techniques, namely, current-voltage and capacitance-voltage methods are described.

2.1.2 Schottky Barrier Formation

Ideally, MS contacts can be classified as either rectifying (allows current to pass in one direction) or ohmic (allows current to pass in either direction) depending on their interface characteristics. However, practical contacts are neither perfectly rectifying nor perfectly ohmic. In MS contacts, current transport is primarily due to majority carriers, unlike in a p-n junction, where minority carriers constitute the bulk of the current [6]. MS junctions are characterised by their SBH denoted by $q\phi_{Bn}$ or $q\phi_{Bp}$ for metal/n-type semiconductor and metal/p-type semiconductor contacts, respectively.

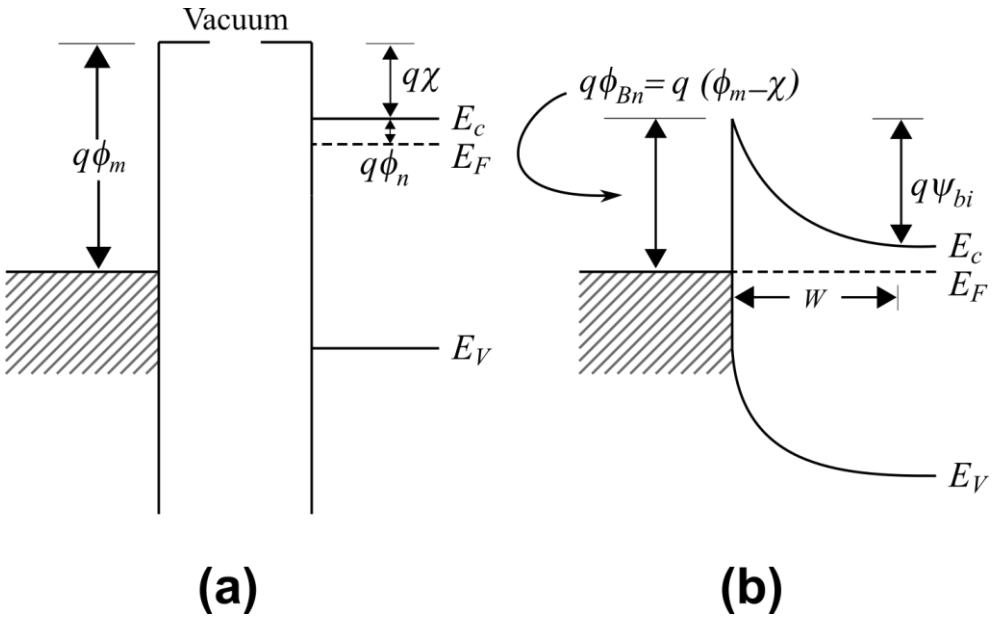

Figure 2.1: The formation of a Schottky barrier between a metal and an n-type semiconductor, (a) neutral and isolated states and (b) in perfect connection after reaching thermal equilibrium (redrawn after ref. 6).

This barrier, extending across a region fully depleted from mobile charge carriers with width W [µm] in the semiconductor, is formed when a metal is placed in contact with a semiconductor at the MS interface, as shown in Figure 2.1 (b).

When a metal is placed in contact with a semiconductor, a potential barrier is formed at the MS interface. The Fermi level of the metal must aligns with the Fermi level of the semiconductor at thermal equilibrium. According to the Schottky-Mott model, the barrier height of an ideal metal/n-type semiconductor Schottky contact is equal to the difference between the metal work function $q\phi_m$ (the energy required to liberate an electron from the material to the vacuum level) and the electron affinity $q\chi$ of a semiconductor (the energy released when an electron is added to the material), which can be written as [6]:

$$q\phi_{Bn} = q(\phi_m - \chi)\ [eV] \qquad (2.1)$$

For an ideal metal/p-type semiconductor Schottky contact:

$$q\phi_{Bp} = E_g - q(\phi_m - \chi)\ [eV] \qquad (2.2)$$

The height of the barrier relative to the conduction band position in the neutral region of the semiconductor is called the built-in potential (also called diffusion potential), $q\psi_{bi}$, can be expressed as:

$$q\psi_{bi} = q(\phi_{Bn} - \phi_n)\ \ [eV] \qquad (2.3)$$

$$q\psi_{bi} = q(\phi_{Bp} - \phi_{p)}\ \ [eV] \qquad (2.4)$$

where $\phi_n = (E_c - E_F)/q$ [V] and $\phi_p = (E_F - E_V)/q$ [V] are Fermi potentials from conduction-band edge and valence-band edge in n-type and p-type semiconductor, respectively. In Figure 2.1 (b), a built-in potential $q\psi_{bi}$ can observed across the MS contact under equilibrium.

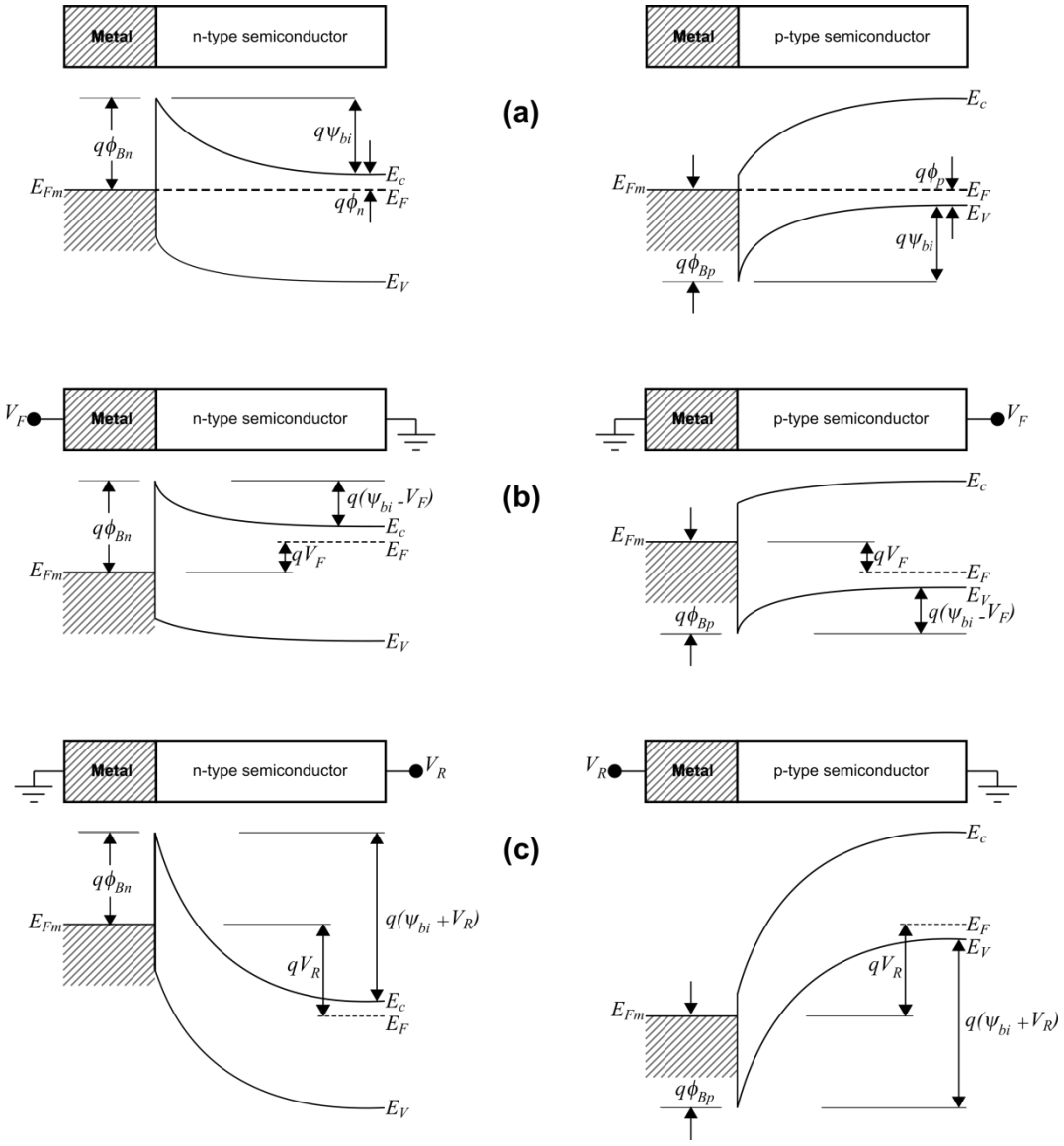

Figure 2.2: Energy-band diagrams of M/n-type (left) and M/p-type (right) semiconductor contacts, (a) thermal equilibrium, (b) under forward bias, and (c) under reverse bias (redrawn after ref. 6).

When a forward bias voltage, V_F, is applied, electrons in the metal side have to overcome a greater potential energy barrier, $q\phi_{Bn}$, to enter the conduction band of the n-type semiconductor compared to the conduction-band-electrons in the n-type semiconductor which have to overcome a smaller barrier $q(\psi_{bi} - V_F)$ to enter the metal. The same concept applies to the semiconductor's valence-band holes in a metal/p-type semiconductor contact configuration. The energy-band diagrams for metals on n-type (left) and p-type (right) semiconductors under different biasing conditions are shown in Figure 2.2.

The spatial distribution of the potential, electric field, junction capacitance, and the depletion layer width can be determined by solving Poisson's equation in the space-charge region under the abrupt approximation (i.e. total charge density $\rho \approx qN_D$ for x < W, $\rho \approx 0$ and the electric field $F \approx 0$ for x > W), where q is the electron charge and N_D is the carrier density for n-type semiconductor. Given that ε_s is the permittivity of the semiconductor, at equilibrium, the width of the depletion layer W can be written as:

$$W = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{qN_D}} \qquad (2.5)$$

When an external bias voltage V_A is applied on the contact, the depletion region W can be expressed as:

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(\psi_{bi} - V_A - \frac{kT}{q}\right)} \qquad (2.6)$$

where *k* is the Boltzmann's constant and *T* is the temperature [K]. The electric field $|F(x)|$ [V/cm] is a function of the junction depth and can be expressed in terms of the maximum electric field F_{max} which occurs at x=0:

$$|F(x)| = \frac{qN_D}{\varepsilon_s}(W - x) \qquad (2.7)$$

$$|F(x)| = F_{max} - \frac{qN_D x}{\varepsilon_s} \qquad (2.8)$$

$$F_{max} = \sqrt{\frac{2qN_D}{\varepsilon_s}\left(\psi_{bi} - V_A - \frac{kT}{q}\right)} \qquad (2.9)$$

$$F_{max} = \frac{2\left[\psi_{bi} - V_A - \frac{kT}{q}\right]}{W} \qquad (2.10)$$

These equations will be recalled later in subsection 2.1.3 describing current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) measurements.

An ohmic contact is a metal-semiconductor contact that has a negligible contact resistance R_C relative to the total resistance of the semiconductor device [6]. The specific contact resistance ρ_C is defined as the reciprocal of the derivative of the current density with respect to the voltage across the interface at zero bias and can be written as

$$\rho_C = \left(\frac{dJ}{dV}\right)^{-1}_{V=0} \ [\Omega\ \mathrm{cm}^2] \qquad (2.11)$$

where J is the current density and V is the applied voltage. Essentially, the voltage drop across the ohmic contact should be small when compared to the voltage drop across the active region of the device.

In MS contacts, current transport is primarily due to majority carriers, unlike in a p-n junction, where the minority carriers are responsible. There are five carrier transport mechanisms that can occur in Schottky barriers in the forward-biased direction illustrated in Figure 2.3 [6]. These mechanisms are:

1) Thermionic emission over the potential barrier into the metal (the dominant current mechanism in forward-biased Schottky contacts with moderately doped semiconductors (N_D or $N_A \leq 10^{17}$ cm^{-3}),
2) Quantum-mechanical tunnelling through the barrier (important for heavily doped semiconductors and accountable for most ohmic contacts),
3) Recombination and/or generation in the space-charge region,
4) Diffusion of majority carriers in the depletion region, and
5) Diffusion of minority carriers injected from the metal into the semiconductor (equivalent to recombination in the neutral region).

Ideally, the *I-V* characteristics of Schottky diodes can described by assuming that current transport is dominated by thermionic emission over the potential barrier into the metal and can be expressed mathematically as [6]:

$$I = I_s\left(e^{qV/kT} - 1\right) \qquad (2.12)$$

$$I_s = AA^*T^2e^{-q\phi_B/kT} \qquad (2.13)$$

where A [cm^{-2}] is the diode area, A^* is the effective Richardson constant ≈110 A/cm^2-K^2 for n-type Si and 30 A/cm^2-K^2 for p-type Si, ϕ_B (ϕ_{Bn} or ϕ_{Bp}) [V] is the Schottky barrier height, and I_s is the reverse-bias saturation current.

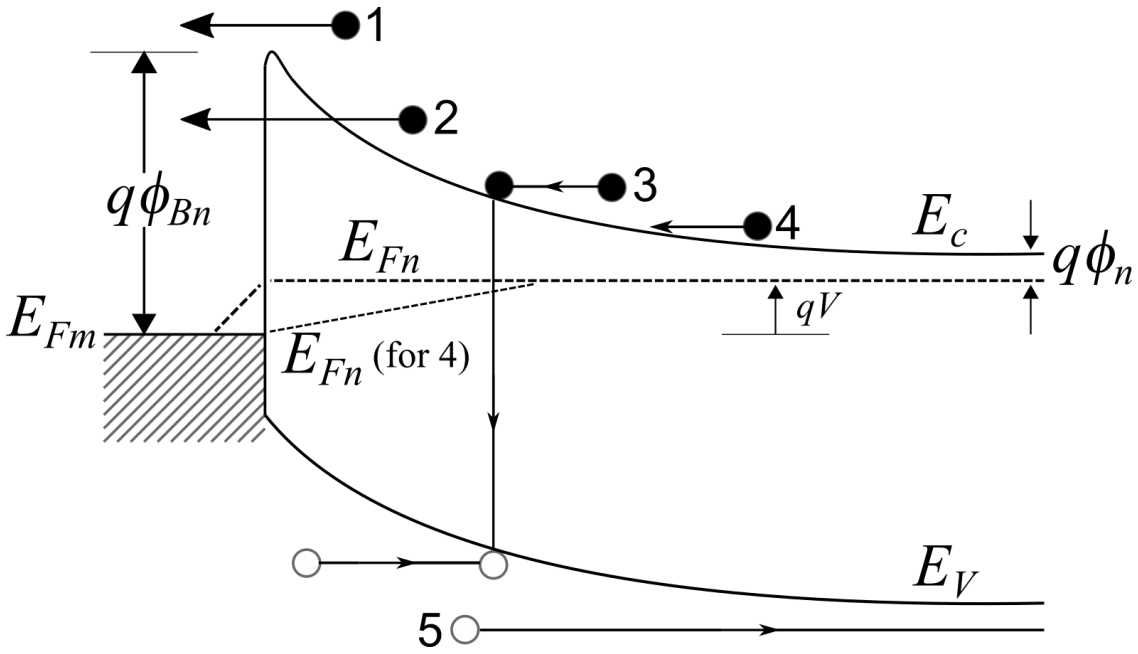

Figure 2.3: Current transport mechanisms (redrawn after ref. 6).

2.1.3 Practical MS Contacts and Barrier Height Measurements

Due to the presence of interface states at the MS interface and an interfacial layer between the surfaces of the metal and semiconductor (e.g. an insulating silicon dioxide (SiO_2)), an agreement between equations (2.1) or (2.2) and experimental measurements is rare [6]. Also, practically, ϕ_m is not constant because of its high sensitivity to surface contamination. In real Schottky diodes, the value of ϕ_{Bn} or ϕ_{Bp} is not independent of the applied bias but instead, it decreases as the applied bias increases (a phenomenon known as Schottky-barrier lowering). The diode ideality

factor n is a constant introduced to equation (2.12) to account for experimentally-observed deviations from the ideal theory with typical values ranging from 1 to 2. For practical Schottky diodes, equation (2.12) becomes:

$$I = I_s\left(e^{qV/nkT} - 1\right) \quad (2.14)$$

For $V>3kT/q$, equation (2.14) can be reduced to $I = I_s e^{qV/nkT}$. The value of n depends on the fabrication process and the quality of materials used for fabricating Schottky diodes. For example, diodes fabricated by epitaxially-grown metals on rigorously-cleaned semiconductor surfaces will have improved values of n compared to others fabricated by conventional metal-evaporation processes.

Values of I_s, n, and ϕ_B can be determined practically by current-voltage (*I*-*V*) measurements. Assuming a uniform semiconductor doping profile and current transport due to thermionic emission, the values of n and I_s can be extracted from the slope and zero voltage intercept of the closest straight line fit to a ln(*I*) versus *V* plot. The value of the barrier height can then be obtained from equation (2.13):

$$\ln(I) = \ln(I_s) + \frac{q}{nkT}\,V \quad (2.15)$$

$$n = \frac{q}{kT}\left(\frac{dv}{d(lnI)}\right) \quad (2.16)$$

$$\phi_B = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_s}\right) \quad (2.17)$$

In addition, from capacitance-voltage (*C*-*V*) measurements, the $1/C^2$ versus *V* plot for reverse bias and moderate forward bias is used to calculate the values of the built-in potential ψ_{bi} (intercept on the *V* axis), carrier density N_A for p-type Si or N_D for n-type Si (slope of the straight line), and consequently barrier height ϕ_B. For a metal/n-Si Schottky diode:

$$N_D = \frac{2}{q\epsilon_s}\left[-\frac{1}{d(1/C_D^2)/dV}\right] \quad (2.18)$$

$$\phi_{Bn} = \psi_{bi} + \phi_n + \frac{kT}{q} - \Delta\phi \quad (2.19)$$

where C_D is the depletion-layer capacitance per unit area and $\Delta\phi$is the image-force lowering. Differences between barrier heights derived from *C-V* and *I-V* measurements are often attributed to the presence of interface layers, inhomogeneous doping, and/or surface damage [6].

2.2 Numerical Modelling of Semiconductor Devices

The behaviour of any semiconductor device whether it is electrical, optical, or thermal can be modelled numerically if the following requirements are satisfied:

1) A complete set of device-physics equations that governs the behaviour of interest are formulated.
2) The boundary conditions relevant to the operation of the device are known or can be derived.
3) A robust solving method is employed.

These requirements have led to the emergence of *Computational Electronics*; a field of research referring to the physical simulation of semiconductor devices in terms of charge transport and the corresponding electrical behaviour [22, 23]. Numerous studies have been devoted to utilising the ever-growing computational resources in modern computers for semiconductor device simulations. However, the speed-accuracy dilemma has always been a critical matter since the early days of semiconductor device simulations. The main objective of this field is to provide

TCAD tools with time-efficient simulation techniques capable of capturing the essential physics and obtaining results within a reasonable timeframe.

Nowadays, there are a number of commercial TCAD tools that can accommodate all the aforementioned requirements. However, the simulation results are only as accurate as the physics (or physical models) used to simulate the behaviour of the device. Therefore, it is essential to choose the correct physics in a TCAD tool to obtain reliable simulation results.

Device-physics equations often appear in the form of partial differential equations (PDEs). TCAD tools employ Finite Element Method (FEM) to numerically discretise the relevant PDEs within the simulation domain. In other words, the device structure is approximated by a simulation grid (or mesh) that contains a finite number of discrete 'mesh' elements. Next, by applying boundary conditions, the device simulator (i.e. numerical solver) solves the discretised equations at each grid point to calculate and record the values of the device variables (e.g. doping concentrations, carrier concentrations, and electrostatic potential) at each grid point. Examples of boundary conditions include electrical boundary conditions such as the type of electrodes (i.e. ohmic or Schottky) and applied bias or thermal boundary conditions such as thermal conduction across interfaces. The subsequent section briefly reviews the framework used in Sentaurus TCAD by SYNOPSYS [24, 25] to perform semiconductor device simulations. The physics implemented, particularly the Drift-Diffusion (D-D) transport model is highlighted. Details of interfacial boundary conditions and key built-in models used in the M-R-S approach such as mobility, Schottky barrier lowering, and distributed contact resistance will be discussed in chapter 4.

2.3 TCAD Simulation Procedure

A depiction of Sentaurus TCAD modelling stages and tool flow can be seen in Figure 2.4. The Sentaurus Workbench (SWB) environment represents the outer layer of the Sentaurus suite that connects and manages the operations necessary for the simulation study. It has an interactive Graphical User Interface (GUI) that is capable of automatically running a number of prescheduled simulation scenarios. This is a key feature in TCAD as it enables the user to study the effect of varying each parameter in a model over a wide range of values. Two main tools are used within SWB to build models and perform simulations; Sentaurus Structure Editor (SDE) and Sentaurus Device (SDEVICE).

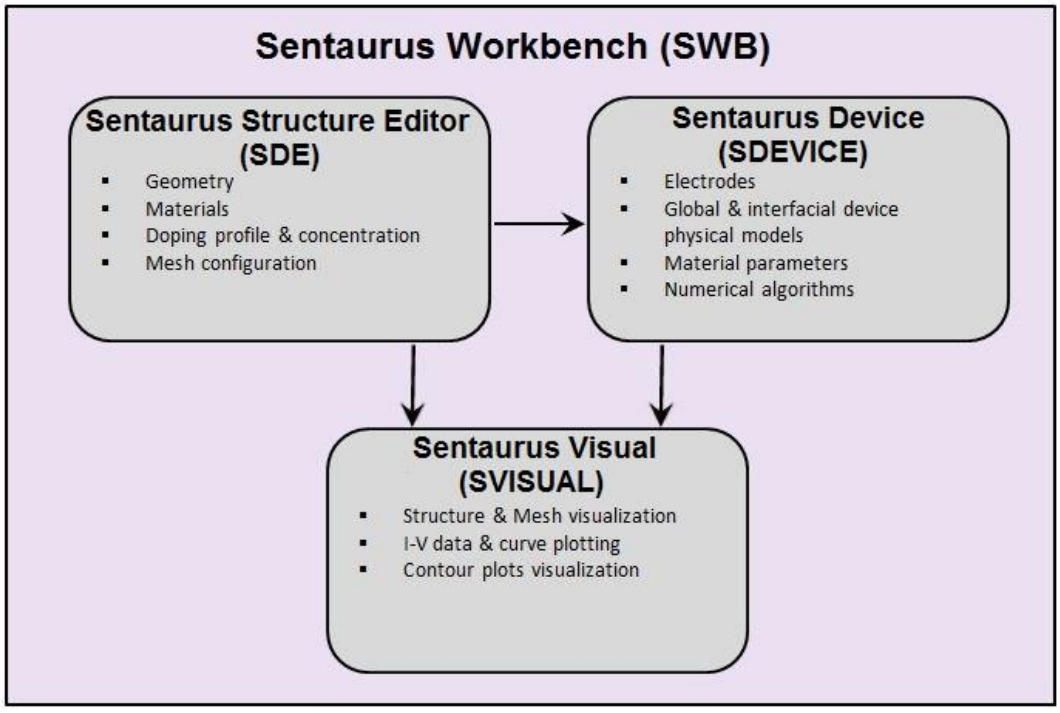

Figure 2.4: Overview of TCAD's tools flow, order of use, and summery of the main tasks performed in each tool.

2.3.1 Sentaurus Structure Editor (SDE)

SDE is used to generate the physical structure of the device. It is powered by an interactive GUI with a small command-line window. The user can create complete virtual 2D/3D devices by either drawing geometrical boundaries or writing script-based commands. Alternatively, users can copy/paste or load input files (which were previously written on a standard text editor) that contain all the required commands to successfully generate the desired device. The scripting language of SDE is based on Scheme programing language. Rectangles, circles, cuboids, polygons, cylinders, and spheres can be drawn and edited in 2D/3D coordinate system. Editing includes moving, deleting, and cutting 2D/3D boundaries in addition to chamfering and rounding 2D/3D edges. Each boundary or 'region' (as TCAD refers to it) is defined by a name, a position, and a material type. The position of a 2D/3D region is defined by two coordinate points (x_1, y_1, 0) & (x_2, y_2, 0) for 2D boundaries and (x_1, y_1, z_1) & (x_2, y_2, z_2) for 3D boundaries. In TCAD, materials are categorised as either conductors (e.g. metals and metal silicides), semiconductors (e.g. Si and Ge), or insulators (e.g. SiO_2 and Si_3N_4). TCAD provides users with an extensive list of materials to choose from. Each material has a parametric file (.par) where its properties are defined. New materials can also be created in TCAD. For semiconductor regions, doping profiles can be either constant or analytic and the user can specify the doping species and doping concentration. Meshing strategy is also defined in this tool. Mesh elements can be either triangular or rectangular in 2D and tetrahedral in 3D. TCAD has three different meshing engines: Mesh, SNMesh, and NOffset3D. Each one has its own benefits and drawbacks depending on the modelled geometry.

2.3.2 Sentaurus Device (SDEVICE)

SDEVICE is used to simulate the electrical behaviour of the samples by incorporating semiconductor device physics and numerical methods to solve for the variables of interest (e.g. terminal voltages and currents). The framework of simulation depends on the type of carrier transport model adopted. For the Drift-Diffusion (D-D) model, TCAD starts the electrical simulation by computing the spatial distribution of three variables; the electron carrier density n [cm^{-3}], the hole carrier density p [cm^{-3}], and the electrostatic potential ψ [V]. For steady-state simulation, the relations between these key quantities are described by a system of three fundamental semiconductor equations. The equations are the Poisson, the electron continuity equation, and hole continuity equation. These equations can be written in the following form:

Poisson's equation: $$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D - N_A) - \rho_{trap} \quad (2.20)$$

Electron continuity equation: $$\nabla \cdot \overrightarrow{J_n} = qR_{net,n} + q\frac{\partial n}{\partial t} \quad (2.21)$$

Hole continuity equation: $$-\nabla \cdot \overrightarrow{J_p} = qR_{net,p} + q\frac{\partial p}{\partial t} \quad (2.22)$$

where:

ε [Farad cm^{-1}] is the electrical permittivity and can be expressed as $\varepsilon = \varepsilon_o \varepsilon_r$;

ρ_{trap} [cm^{-3}] is the charge density contributed by traps and fixed charges;

$\overrightarrow{J_n}$ [A cm^{-2}] is the current density of electrons;

$\overrightarrow{J_p}$ [A cm^{-2}] is the current density of holes; and

$R_{net,n}$ and $R_{net,p}$ are the net recombination rate [cm^{-3} s^{-1}] for electrons and holes accounting for activated generation (G) and recombination (R) processes in the simulation and can be expressed as $R_{net} = R - G$.

The electron and hole densities p and n can be computed from the electron and hole quasi-Fermi potentials. Assuming Fermi statistics:

$$n = \gamma_n N_C \left(\frac{E_{Fn} - E_C}{kT}\right) \qquad (2.23)$$

$$p = \gamma_p N_V \left(\frac{E_v - E_{Fp}}{kT}\right) \qquad (2.24)$$

where:

N_C and N_V are the effective density of conduction and valence band states [cm^{-3}];

$E_{Fn} = -q\psi_n$ and $E_{Fp} = -q\psi_p$ are the quasi-Fermi energies for electrons and holes [eV];

ψ_n and ψ_p are the quasi-Femi potentials for electrons and holes [V]; and

E_C and E_v are conduction and valence band energy edges [eV] defined as:

$$E_C = -\chi - q(\psi - \psi_{ref}) \qquad (2.25)$$

$$E_v = -\chi - E_{g,eff} - q(\psi - \psi_{ref}) \qquad (2.26)$$

where:

χ is the electron affinity of the semiconductor;

ψ_{ref} [V] is a reference potential that can be expressed as $\psi_{ref} = \psi_i$ in devices containing silicon (ψ_i [V] is the intrinsic Fermi level); and

$E_{g,eff}$ [eV] is the effective bandgap (i.e. after narrowing the bandgap E_g by E_{bgn})

In TCAD, using the *OldSlotboom* bandgap narrowing model, $E_{g,eff}$ is modelled as a function of lattice temperature *T*:

$$E_{g,eff}(T) = E_g(T) - E_{bgn} \quad (2.27)$$

$$E_{g,eff}(T) = E_{g,0} + \delta E_{g,0} - \frac{\alpha T^2}{T+\beta} - E_{bgn} \quad (2.28)$$

The electron affinity of silicon χ is temperature-dependant and affected by bandgap narrowing:

$$\chi(T) = \chi_0 + \frac{(\alpha+\alpha_2)T^2}{2(T+\beta+\beta_2)} + bgn2chi \cdot E_{bgn} \quad (2.29)$$

The default values for the bandgap narrowing parameters in eq. (2.28) and eq. (2.29) are summarised in Table 2.1 for silicon. The reader can refer to ref. [25] for a detailed explanation about other bandgap narrowing models and the corresponding fitting parameters.

In eq. (2.23) and eq. (2.24), γ_n and γ_p can be computed as:

$$\gamma_n = \frac{n}{N_c} e^{\left(\frac{E_c - E_{Fn}}{kT}\right)} \quad (2.30)$$

$$\gamma_n = \frac{n}{N_v} e^{\left(\frac{E_{Fp} - E_v}{kT}\right)} \quad (2.31)$$

The diffusivities of electrons D_n [cm^2/s] and holes D_p [cm^2/s] can be expressed in terms of the mobilities of electrons μ_n [cm^2/Vs] and holes μ_n [cm^2/Vs]:

$$D_n = kT\mu_n \qquad (2.32)$$

$$D_p = kT\mu_p \qquad (2.33)$$

Table 2.1: Default *OldSlotboom* bandgap narrowing parameters for silicon [25].

Parameter	Default Value	Unit
$E_{g,0}$	1.1696	eV
$\delta E_{g,0}$	-1.595×10^{-2}	eV
α	4.73×10^{-4}	eV/K
α_2	0	eV/K
β	636	K
β_2	0	K
χ_0	4.05	eV
$bgn2chi$	0.5	1
E_{bgn}	9.0×10^{-3}	eV

The current densities for electrons $\overrightarrow{J_n}$ [A/cm^2] and holes $\overrightarrow{J_p}$ [A/cm^2] can be expressed as:

$$\overrightarrow{J_n} = -nq\mu_n \nabla\psi_n \quad (2.34)$$

$$\overrightarrow{J_p} = -nq\mu_p \nabla\psi_p \quad (2.35)$$

For boundary conditions at material interfaces, the displacement current density $\overrightarrow{J_D}$ is always included to ensure current conservation. In SDEVICE, the total current density $\vec{J}$ is written as:

$$\vec{J} = \overrightarrow{J_n} + \overrightarrow{J_p} + \overrightarrow{J_D} \quad (2.36)$$

SDEVICE simplifies the band structure of semiconductor materials to four quantities: the conduction band energy edge E_C, the valence band energy edge E_v (or, alternatively, the temperature-dependant bandgap energy $E_g(T)$ and electron affinity $\chi(T)$), the density-of-states (DOS) effective mass for electrons m_n, and the DOS effective mass for holes m_p (or, alternatively, the effective DOS for electrons in the conduction band $N_C(m_n, T_n)$ and the effective DOS for holes in the valence band $N_V(m_p, T_p)$). For Silicon, these quantities are modelled as follows:

1) Effective mass and conduction band edge DOS for electrons

$$m_n = 6^{2/3}(m_t^2 m_l)^{1/3} + m_m \quad (2.37)$$

$$\frac{m_t(T)}{m_0} = a\frac{E_g(0)}{E_g(T)} \quad (2.38)$$

$$N_C(m_n, T_n) = 2.5094 \times 10^{19}\left(\frac{m_n}{m_0}\right)^{3/2}\left(\frac{T_n}{300\ K}\right)^{3/2} cm^{-3} \quad (2.39)$$

where:

$m_t(T)$ is the temperature-dependent effective mass component;

m_0 is the electron rest mass [kg]; and

a= 0.1905, m_l= 0.9163, and m_m= 0.0 are the default coefficients for eq. (2.37) and eq. (2.38).

2) Effective mass and valence band edge DOS for holes

$$\frac{m_p(T)}{m_0} = \left(\frac{a + bT + cT^2 + dT^3 + eT^4}{1 + fT + gT^2 + hT^3 + iT^4}\right)^{2/3} + m_m \quad (2.40)$$

$$N_V(m_p, T_p) = 2.5094 \times 10^{19} \left(\frac{m_p}{m_0}\right)^{3/2} \left(\frac{T_p}{300\ K}\right)^{3/2} cm^{-3} \quad (2.41)$$

where:

$a = 0.4435870$; $b = 0.3609528 \times 10^{-2}[\mathrm{K}^{-1}]$; $c = 0.1173515 \times 10^{-3}[\mathrm{K}^{-2}]$; $d = 0.1263218 \times 10^{-5}[\mathrm{K}^{-3}]$; $e = 0.3025581 \times 10^{-8}[\mathrm{K}^{-4}]$; $f = 0.4683382 \times 10^{-2}[\mathrm{K}^{-1}]$; $g = 0.2286895 \times 10^{-3}[\mathrm{K}^{-2}]$; $h = 0.7469271 \times 10^{-6}[\mathrm{K}^{-3}]$; $i = 0.1727481 \times 10^{-8}[\mathrm{K}^{-4}]$; and m_m= 0.0 are the default coefficients for eq. (2.40).

The intrinsic density $n_i(T)$ for undoped semiconductors and effective intrinsic density $n_{i,eff}$ (including doping-dependent bandgap narrowing) are defined as:

$$n_i(T) = \sqrt{N_C(T)N_V(T)}e^{\left(\frac{-E_g(T)}{2kT}\right)} \quad (2.42)$$

$$n_{i,eff} = n_i e^{\left(\frac{E_{bgn}}{2kT}\right)} \quad (2.43)$$

Finally, Sentaurus Visual (SVISUAL) was chosen in order to visualise the structure of the device as well as simulation results.

2.4 Review of Rectifying Carbon/Silicon Devices in Literature

A review highlighting significant literature regarding C/Si Schottky diodes is presented in this section. This review reports key articles reviewing C-Si junctions and summarises experimental studies according to their chronological order of publication.

According to the recent article by Li *et al.* [26], results of the first systematic investigation of C-Si interfaces was presented by Bhagavat *et al.* [27] in 1979. In this investigation, the *I-V* measurements of the structure containing evaporated amorphous carbon films as electrodes on top of n-type Si substrates were conducted under dark and light conditions showing a clear rectifying behaviour and photovoltaic output. They used an arc evaporation technique (details reported in [28]) to evaporate pure graphite in a vacuum of 10^{-5} Torr [27]. The reported diodes' RR was of the order of one hundred. Despite their promising results, the work did not motivate research in C/Si junctions in the following 1980s period due to the immature carbon crystal growth techniques [26].

During the 1990s, a number of researchers investigated the electrical and optical behaviour of devices based on C-Si interfaces with the focus being on realizing current-rectifying devices [29, 31, 34-39]. An early key study in this period reported fabrication of large area Al/C/Si sandwich structures where hard C thin films containing polycrystalline diamond were deposited onto n-type and p-type Si substrates using Radio-Frequency Plasma-Enhanced CVD (RF PECVD) system [29]. The authors cited their previous work for details of C thin films deposition conditions. In their previous work about their C thin film deposition process, they reported that the Si substrate was kept at 20 °C during deposition by pumping coolant through the bottom electrode on

which the Si substrate is placed in the system [30]. The Large area Al/C/Si diodes showed rectifying *I-V* characteristics consistent with the presence of what was treated as C/Si heterojunction because the deposited C thin films were considered as being an intrinsic semiconducting material. The same group conducted similar investigation by fabricating Au/C/Si diodes by depositing C films using vacuum arc deposition system at low temperature instead of RF PECVD [31]. The deposited C thin films were almost entirely tetrahedrally-bonded and the authors referred to them as amorphous diamond (a-diamond). The bandgap of these a-diamond (or ta-C) thin films was determined to be approximately 2.9 eV, which was 0.9 eV higher than C films reported in ref. [29]. Parallel to ref. [29], the authors ascribed the observed rectifying behaviour to the ta-C/Si heterojunction [31]. After refining their formation and successful doping technique to form n-type ta-C thin films using a FCVA system [32-34], V. S. Veerasamy *et al.* [35] were motivated to investigate the n-type ta-C/p-Si heterojunction as a future building block for Heterojunction Bipolar Transistors (HBTs). They reported diode ideality factors *n* ranging from 1.68 to 1.94 obtained at low voltage region. Yu *et al.* [36] achieved an improved ideality factor of 1.10 for the C/n-Si photovoltaic cell. They attributed this relatively low value to the homogenous amorphous structure of their C thin film, made by a CVD of 2,5-dimethyl-p-benzoquinone process at a substrate temperature of 500 °C. The same group presented a detailed investigation about the characteristics of the C/n-Si junction estimating a work function of about 5 eV for the carbonaceous thin film based on the energy band diagram of this junction [37]. Chhowalla *et al*. [38] discussed the influence of ion energy and substrate temperature on the electronic and optical properties of ta-C films deposited using the FCVA system. Konofaos *et al.* [39] ion-implanted hydrogenated amorphous carbon films (a-C:H) with boron and studied the influence of boron doses

on the *I-V* characteristics of Al/a-C:H/n-Si diodes. The C films were grown by PECVD at a constant substrate temperature of 350 °C. They concluded that devices with lower doses of boron behaved as Schottky diodes (i.e. low turn-on voltages and leaky reverse currents) while those with higher boron doses resembled the behaviour of p-n junction diodes.

The majority of C-Si studies in the 1990's era were focusing on fabricating sp^3-rich amorphous C thin films due to their attractive physical and mechanical properties for optoelectronic devices such as transparency and hardness, respectively. After 2004, focus has largely shifted towards other forms of C thin films, particularly graphene derivatives. Nevertheless, the tunable properties of a-C films continue to attract attention and potential applications are being sought [40-42].

A study showing the potential of a-C/Si junctions in gas pressure sensing applications was presented by Gao *et al*. [40]. The authors reported the effect of gas pressure on the sp^2/sp^3 ratio and sp^2 cluster size in these films deposited using direct current magnetron sputtering at room temperature on n-Si. Films were deposited at a pressure of 0.5, 2 and 4 Pa. Observations of Raman spectra of these films suggested that the film deposited at 4 Pa had the strongest sp^2 bonding among the three films. In addition, it had the largest sensitivity to gas pressure based on *I-V* measurements conducted under different gas pressures.

Yap *et al*. [41] reported the effects of laser wavelength (nm) and fluence (J/cm^2) on the C film resistivity deposited on glass using pulsed Nd:YAG laser deposition and discussed the measured *I-V* characteristics of a-C/p-Si junctions for four different

deposition conditions. These conditions are i) 355 nm and 42 J/cm^2, ii) 355 nm and 21 J/cm^2, iii) 1064 nm and 42 J/cm^2 and iv) 1064 nm and 21 J/cm^2. Diamond-like carbon (DLC) films deposited using short wavelength and high fluence laser exhibited the highest sp^3 content and resistivity.

Gupta *et al.* [42] reported *I-V* fabrication and characterisation results of a-C/p-Si diodes fabricated at room temperature and at 200 °C using 248 nm wavelength KrF excimer laser. Raman spectra results suggested disordered DLC characteristics. Values for *n* were estimated at low and high voltage to be 1.12 and 2.32, respectively for junction fabricated at room temperature. They observed a decrease in the values of *n* (1.06 and 2.31, at low and high voltage, respectively) for junctions fabricated at 200 °C. The SBHs values were estimated to be 0.37 and 0.41 for junctions fabricated at room temperatures and 200 °C, respectively. By inspecting the presented *I-V* plots, Au/p-Si/a-C/Au diodes fabricated at 200 °C exhibited the highest RR exceeding two orders of magnitude of rectification at ± 1 V.

The formation of rectifying graphite/n-Si Schottky diodes were first demonstrated by Tongay *et al.* [12] using three "soft landing" deposition techniques. The first Schottky contacts were made by pressing Highly Oriented Pyrolytic Graphite (HOPG) onto the Si substrate (relatively large HOPG ~ 1 mm^2 piece). In the second method, mechanically exfoliated (~ 0.5 mm^2) HOPG sheets were landed on the Si substrate. The authors reported in some occasions the HOPG flakes have flattened out with strong adherence to the substrate due to Van der Waals attraction forces. In the third method, colloidal HOPG was prepared and Si substrates were painted with this and air dried. The same procedure was applied to 4H-SiC and GaAs substrates to

fabricate HOPG/4H-SiC and GaAs junctions. The ideality factors for these devices and pressure-contacts were found to be higher than those prepared by landing cleaved HOPG flakes ($1.12 \leq n \leq 1.50$). For HOPG/n-Si, values of effective SBHs extracted from *I-V* and *C-V* measurements were 0.40 and 0.70 eV, respectively. The authors attributed this difference to the presence of a thin oxide layer at the MS interface causing an additional voltage drop in the *C-V* measurements. RRs exceeding four orders of magnitude were observed for HOPG/n-Si diodes at ± 1 V. This method is not suitable for production due to inaccuracy in positioning of the HOPG flakes and lack of reproducibility in device dimensions.

In 2010, Li *et al.* [43] successfully demonstrated rectification characteristics and photovoltaic output of the first graphene-on-silicon Schottky junction solar cells. Graphene sheets were grown by CVD using Ni films/or foils as a substrate and methane gas as a carbon source. This method involved reaching a temperature of 1000 °C to heat Ni. The graphene sheets were deposited onto patterned n-Si/SiO_2 substrates with Au contacts. Rectification ratios (RRs) of $10^4 \sim 10^6$, an ideality factor $n = 1.57$ and reverse leakage current I_s of 0.05~0.5 μA for a 0.1 cm^2 device were obtained from the dark *I-V* measurements. They estimated a SBH of 0.78 eV based on thermionic emission theory. The un-optimised solar cell efficiencies were up to 1.5%. One year later, Chen [9] presented dark and light *I-V* characterisation results of six diode samples fabricated by depositing mechanically-exfoliated graphene bilayers on n- and p-type Si substrates. The ideality factors were ranging from 4.89 to 7.69 for diodes formed on n-type Si and 29.67 to 33.50 for diodes formed on p-type Si. The graphene-Si contact area was different for each sample. The contact area for the sample exhibiting the lowest ideality factor was 24.2 μm^2. For this sample, the authors estimated a Schottky

barrier height SBH of 0.416 eV at room temperature. A significantly higher ON state current densities were measured in n-Si devices compared to those measured in the p-Si devices; this was one of three reported major differences between graphene/n-Si and graphene/p-Si diodes. On the other hand, graphene/p-Si diodes showed higher RRs than graphene/n-Si diodes. RRs less than two orders of magnitude can be seen by observing the presented semi-log *I-V* plots for devices formed on p-type Si.

Yim *et al*. [44, 45] presented studies of diodes fabricated by depositing glassy carbon from pyrolysed photoresist films (PPF) or by pyrolytic carbon (PyC) on n-type Si. In order to form thin conductive PPF layer onto n-Si wafer, a photoresist with phenolic backbone (AZ nLOF 2070) was spin-coated and annealed at 1000 °C in a furnace for 1 hour. The PyC films, deposited using CVD, were grown in a furnace at 950 °C using acetylene (C_2H_2) as a hydrocarbon source. Raman spectra of both films are nearly identical and suggested highly disordered sp^2 characteristics. The *I-V* measurements were taken from six different carbon/n-Si diodes. The PPF/n-Si SBDs showed average values of 1.29, 0.71 eV, and 53.3 Ω for *n*, SBH, and R_S, respectively. For PyC/n-Si SBDs, average values of 1.44, 0.56 eV, and 50 Ω were reported for *n*, SBH, and R_S, respectively. No specific figures were reported for the RRs of these diodes; however, by inspecting the displayed semi-log *I-V* plots [45], one can approximate a RR of three orders of magnitude for PPF/n-Si diodes and nearly two orders of magnitude for PyC/n-Si diodes at ±4 V.

Ideality factors *n* of ~ 1.08 were found to be the lowest reported values [11, 46] based on a thorough search of C/Si Schottky diodes in recent literature. In order to attain their 'ideal' graphene-silicon junctions (n = 1.08), Sinha *et al.* [11] treated the

surface of Cu foil by etching away ~700 nm using ammonium persulfate solution to minimise the metallic impurities prior to low pressure CVD (LPCVD) growth of graphene monolayers on n-Si substrate. These devices exhibited a high RR approaching six orders of magnitude at ± 1 V. However, there is a prominent increase in the leakage current with reverse bias within the range -1.0 V≤V≤ 0 V. The authors used the same processes (except Cu etching prior LPCVD) to fabricate another set of devices with *n* of ~1.5 and lower RR. The experimentally measured SBH for the best performing devices was 0.62 eV. Stelzer *et al.* [46] reported low *n* of 1.089 for C/n-Si Schottky diodes fabricated by CVD-deposition of graphenic carbon onto cleaned Si. This device replicated the commercial BAT15 structure and exhibited excellent power handling capability when compared with the TiSi-Si junctions normally employed.

Finally, progress in C/Si heterojunction solar cells was reviewed by Li *et al.* [47] and a large body of publications regarding graphene Schottky diodes was later given by Di Bartolomeo [48].

3 Experimental and Measurement Details

This chapter details all the experimental conditions and parameters used in the fabrication and characterisation of C/p-Si and Pt/p-Si Schottky diodes.

3.1 Fabrication Steps

It is essential to ensure that no contamination is present on the surface of the silicon substrates prior to each deposition step. The cleaning routine for the samples is performed at room temperature and is described as follows:

1. Start by rinsing the samples in acetone followed by drying in high purity pressured N_2 gas.
2. Rinse in isopropanol alcohol and then deionised (DI) water followed by drying in N_2.
3. Immerse the samples in buffered hydrofluoric acid and then in DI water.
4. Dry in N_2 gas.

All the samples used in this study were 1 cm x 1 cm square substrates diced from 2-inch (111) Boron-doped silicon wafers with resistivity of 1-2 Ω.cm. The wafers were ~ 500 µm thick and polished on one side.

3.1.1 Formation of Backside Ohmic Contacts

In order to form ohmic contacts on the backside (unpolished side) of the substrates, films of Al with thicknesses of ~ 500 nm were deposited on the backside of the substrates by electron beam evaporation. The Al films were heat-treated using a conventional furnace at 350 °C for 30 seconds in N_2 gas ambient. Titanium (Ti)

pellets were placed above the as-deposited samples to avoid Al surface oxidation. The temperature is monitored using a thermocouple placed just under the sample and close to the resistive-heating element. Figure 3.1 shows an experiment where a sample is being heat-treated.

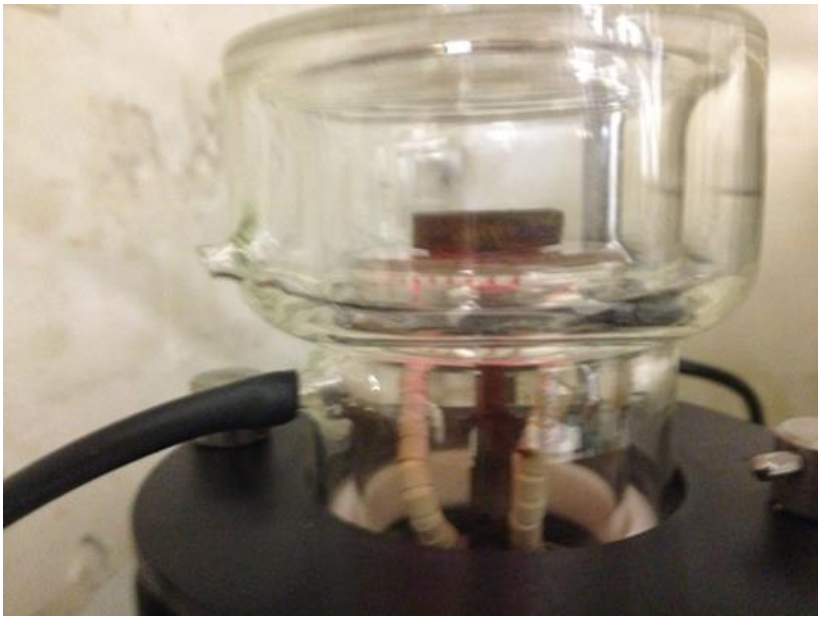

Figure 3.1: Furnace used for heat treatments.

3.1.2 Formation of Front-side Schottky Contacts

For front-side patterning, the samples were spin-coated with AZ1512 photoresist at 3000 rpm for 30 seconds and baked in an oven for 20 minutes at a constant temperature of 90 °C to allow the solvent to evaporate. Next, a mask with patterns of circular apertures with diameters of 400 or 200 µm was aligned using a Karl Suss MJB3 mask aligner and the samples were then exposed to UV light for 8-10 seconds. The patterns were developed in AZ400:DI water (1:4) and the samples were cleaned with DI water and dried before being inspected under an optical microscope to ensure no defects were present.

The energetic carbon deposition process was performed by ablating a 99.99 % carbon cathode (diameter 7 cm) mounted in a Nanofilm Inc. FCVA system. A base pressure of better than 10^{-5} Torr and an arc current of ~ 60 A were used in this process. This FCVA system is fitted with a double-bend magnetic filter which guides the energetic plasma to the substrate and reduces the presence of macroparticles in the deposited films. The FCVA system used for carbon depositions is shown in Figure 3.2 (a) and a schematic illustration of the system components is presented in Figure 3.2 (b).

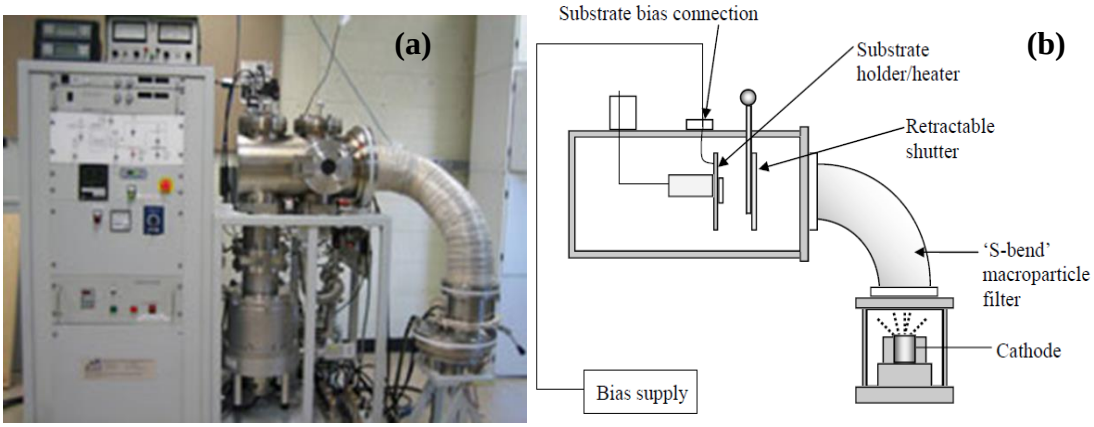

Figure 3.2: (a) Photo of the FCVA energetic deposition system used for carbon depositions (after ref. 49). (b) Schematic illustration of the FCVA energetic deposition system showing its main components (after ref. 50).

The samples were mounted on the substrate holder/heater. The temperature of the substrate holder is controllable and can be varied up to 600 °C. For carbon depositions, a constant DC bias ranging from -0.025 kV to -1.0 kV can be applied to the substrate holder using the regulated DC bias supply shown in Figure 3.2 (b). The bias (kV) to energise the ionised species (carbon ions) for deposition with the FCVA system was varied to form Schottky diodes (with the Schottky junction being the carbon-to-silicon region). The films of carbon were deposited at i) -0.5 kV and 25 °C and ii) -1.0 kV and 100 °C. The energy and temperature of deposition were selected

from parameters known to form rectifying C/n-SiC contacts [50]. A capping layer of ~ 30 nm of Ag was deposited on the carbon by electron beam evaporation to ensure an equipotential is across the Schottky electrode during electrical measurements and also to enhance the visibility of the contacts for probing. Finally, a photoresist lift-off procedure was performed to define the patterned array of 48 circular electrodes. Figure 3.3 presents a summary of fabrication stages.

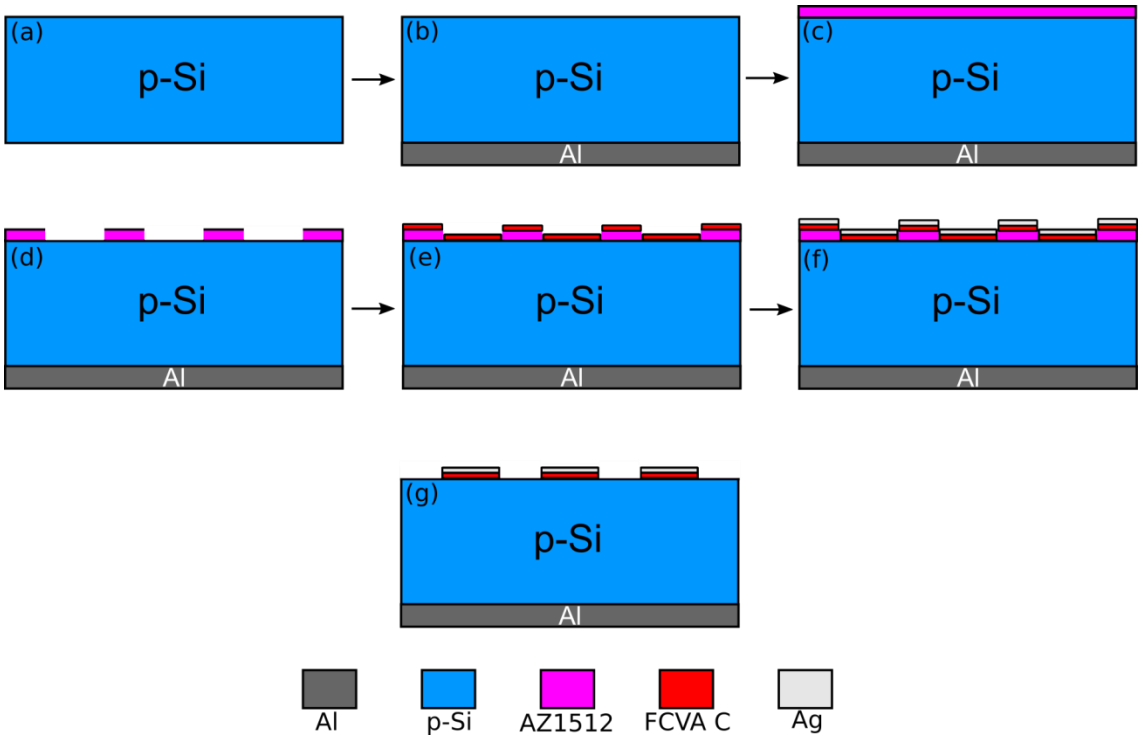

Figure 3.3: Schematic cross sections showing summery of formation stages of three FCVA C/p-Si Schottky diodes (portion of the sample) starting from (a) to (f), part (g) shows the result after the lift-off procedure.

The lift-off procedure used to define the patterned contacts is a very critical fabrication stage. It starts by carefully placing the sample in the bottom of a beaker containing a generous amount of acetone for ~ 24 hours. The sample must be completely submerged in acetone during this time. This step is crucial to ensure penetration of the acetone into the photoresist in order to assist in the lift-off

procedure. The beaker was carefully sealed with aluminium foil to prevent the acetone from being evaporated. The sample was then removed from the beaker and carefully rinsed with pure alcohol without agitation. A 3-D schematic diagram showing a portion of a fabricated sample is presented in Figure 3.4.

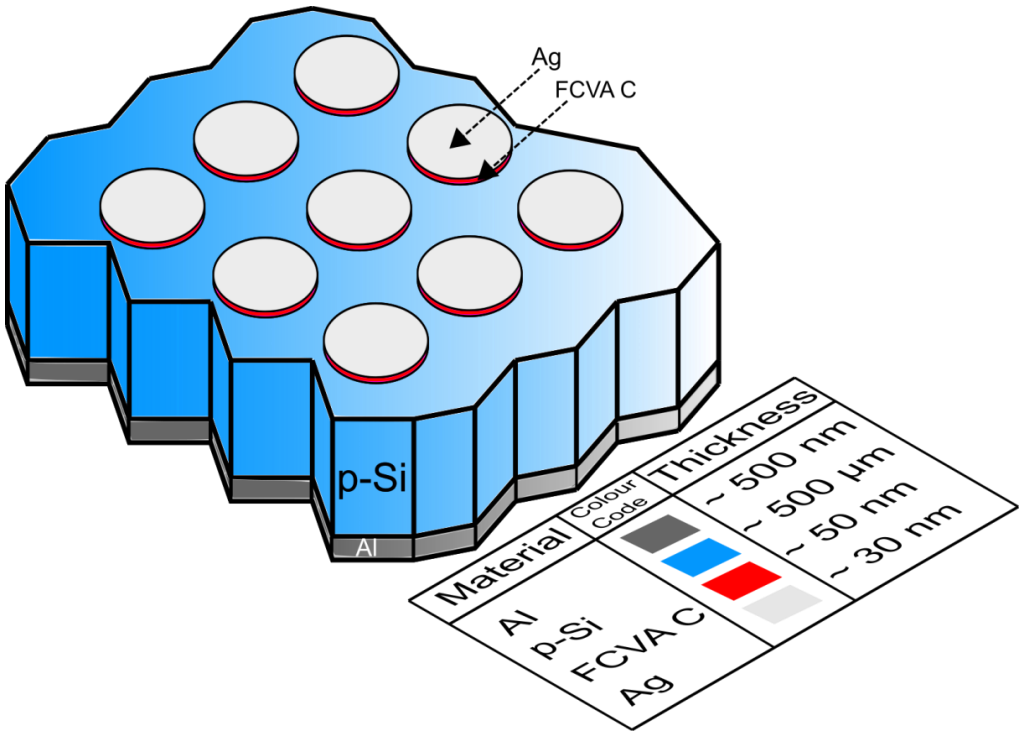

Figure 3.4: 3-D Schematic diagram showing details of materials and thicknesses in a portion of a fabricated sample (nine FCVA C/p-Si Schottky diodes are shown).

For comparison, Pt/p-Si diodes were prepared using the same p-Si wafer described earlier. Thin films of Pt with nominal thicknesses of ~ 15 nm were deposited on the front-side of Si substrates by ion beam sputtering system.

3.2 Electrical Characterisation

Electrical characterisation was performed in order to assess the junction quality and extract the Schottky diode's parameters (i.e. rectification ratio, barrier

height, reverse saturation current, ideality factor, and series resistance) from *I-V* and *C-V* measurements. Also, Hall effect measurements were performed to accurately measure the carrier density and mobility within the substrate.

3.2.1 Current-Voltage (*I-V*) Measurements

The *I-V* curves of the Schottky diodes were obtained by varying the voltage across the junction and measuring the resulting current using a Keithley 2410 SourceMeter. In order to ensure precise probe placement, micromanipulators were used to control the movement of the probe tips in the x, y, and most importantly z direction to prevent damaging the surface of the contacts when the probe tip lands on it during measurements. The *I-V* characterisation was performed at room temperature under an optical microscope with a maximum magnification of ×250 and using two micromanipulator-controlled probes. The supplied current was limited to 10 mA and the *I-V* data were observed on a PC connected to the source meter using the LabTracer software supplied by Keithley Instruments Inc.

3.2.2 Capacitance-Voltage (*C-V*) Measurements

The $1/C^2$-*V* curves of the Schottky diodes were obtained by varying the reverse bias voltage (ac small-signal was superimposed on the reverse bias dc voltage with measurement frequency of 1 MHz) across the junction and measuring the resulting (dark) capacitance using a Boonton 7200 Capacitance Meter. The *C-V* characterisation was performed at room temperature using the same probing/microscope setup described above. The capacitance associated with the probes/cables was de embedded prior to measurement.

3.2.3 Hall Effect Measurements

Room temperature Hall effect measurements were performed using an Ecopia HMS-3000 Hall Effect Measurement System. These measurements were performed to reveal the carrier density in the p-Si. The carrier mobility was also obtained and served as a substrate quality indicator. A square p-Si substrate (from the same wafers used for sample fabrication) was cleaned and four ohmic contacts A, B, C, and D were formed on the corners of the substrate in Van der Pauw configuration (Figure 3.5).

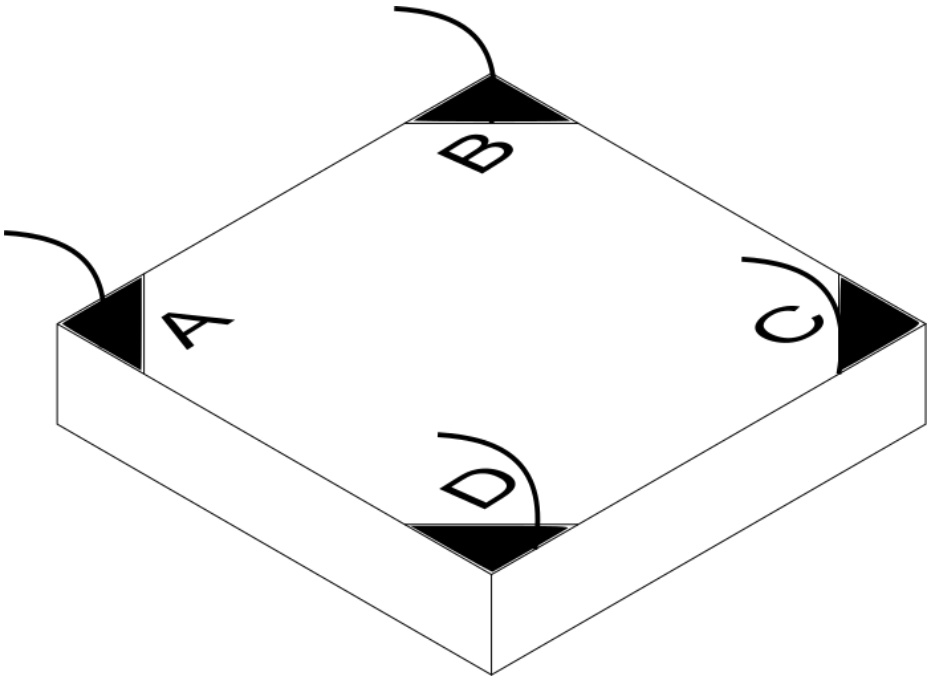

Figure 3.5: Ohmic contacts configuration on the p-Si sample used for Hall effect measurements.

The sample shown in Figure 3.5 is bonded to a mounting board that is inserted between permanent magnets that produce a fixed magnetic field strength of 0.55 T. The magnets can be inserted in forward and reverse directions. The holder is connected to a PC where dedicated software is used to conduct the measurements.

After inputting the desired range of current (1 nA – 20 mA), temperature, and thickness of the sample for measurements, the system automatically conducts current and measures voltages between the contacts. The measurements were started by inspecting *I-V* curves between the contact combinations (I_{AB}-V_{AB}, I_{BC}-V_{BC}, I_{CD}-V_{CD}, I_{DA}-V_{DA}, … etc). All the *I-V* curves were linear indicating that all the contacts were ohmic. This ensured accurate Hall measurements. Next, the system measures and records Hall voltages with zero applied field and with (0.55 T) applied field perpendicular to the sample surface in opposing directions. From these measurements, the carrier concentration and mobility are then calculated.

4 Metal-Resistor-Semiconductor (M-R-S) TCAD Simulations

This chapter presents the Metal-Resistor-Semiconductor (M-R-S) based modelling approach, investigated using Sentaurus TCAD from Synopsys. 2-D and 3-D models were utilised to simulate the electrical behaviour of carbon/p-Si diodes. Most importantly, it describes how this TCAD approach captures the resistive effects observed in the I-V characteristics of the fabricated diodes.

4.1 Introduction

The Metal-Resistor-Semiconductor (M-R-S) TCAD modelling approach was developed to investigate the *I-V* characterisation of the fabricated diodes. The primary feature in the M-R-S structure is the definition of an interface (due to carbon/Si mixed interfacial layer, observed experimentally) between the metal and semiconductor regions to include the effects of added resistance at and near the C-Si junction and barrier lowering. Some physics models were global (e.g. mobility) for the diode structure and others were specific to the interface. In addition to effective metal work function $q\phi_m$ calibration, the value of distributed contact resistance R_D (Ω cm^2), a key parameter in this alternative structure, was selected in order to accurately model part of the resistive effect observed in the *I-V* characteristics of the diodes. Another important aspect of this careful selection of physics models is the inclusion of the Barrier Lowering (BL) effect.

Prior to the M-R-S structure, the *I-V* characterisation of the fabricated diodes was investigated in 2-D using a Metal-Insulator-Semiconductor (M-I-S) structure where the interfacial layer was considered as an insulator. The simulations were

conducted to estimate the effective metal work function $q\phi_m$ and the thickness of an interfacial mixed layer to approximate the experimental results. In a later stage of this thesis work, results of cross-sectional Transmission Electron Microscopy (XTEM) analysis revealed that no discernible native oxide layer was present in the diode sample formed at -1.0 kV and 100 °C, prompting TCAD investigation based on an M-R-S structure where R is likely due to the carbon/Si mixed interfacial layer of ~3 nm observed by XTEM.

In the M-R-S work, two modes of simulation (2-D and 3-D) were utilised to simulate the electrical behaviour of the diodes. The latter was performed to confirm the findings of the former. A detailed description of the M-R-S diode structure in 2-D and in 3-D simulated using Sentaurus TCAD, and its key parameters ($q\phi_m$, R_D, and BL) will be presented in the following sections.

4.2 M-R-S Diode Structure and Mesh Generation

The Sentaurus Structure Editor (SDE) tool was used to generate the M-R-S diode structures for 2-D and 3-D simulations. The details of geometry, materials, and contacts for the 2-D diode structure generated in this study are shown in Figure 4.1. For the 3-D simulation mode, a ⅛ section of the full diode structure was generated as illustrated in Figure 4.2. The models consist of Schottky electrode contacts with thickness of 50 nm on 500 µm thick Boron-doped Si and ideal ohmic contacts covering the top of the metal and bottom of Si substrate, with zero resistance. A uniform carrier concentration of 8×10^{15} cm^{-3} was defined for the Si substrates, in accordance with the Hall effect measurements.

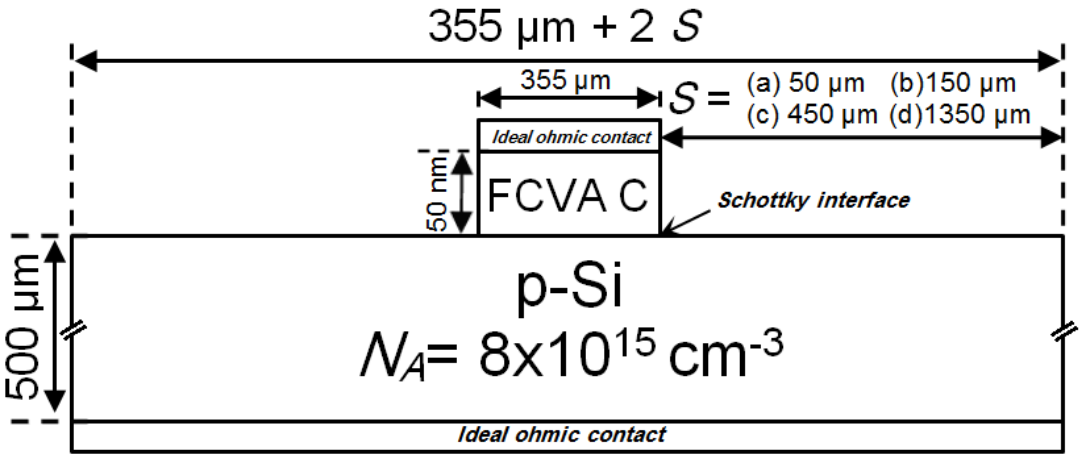

Figure 4.1: Schematic representation of the cross section of the 2-D M-R-S diode structure generated in Sentaurus TCAD showing the details of geometry, materials, and contacts.

For 2-D simulation mode, the contact width is 355 µm while the Si width is variable (355 + 2*S* µm; where *S* is the length of Si extending laterally beyond the Schottky contact edge). The purpose of varying *S* was to determine the length (*S*) of silicon extending beyond the contact, beyond which any increase in *S* makes no difference to the electrical characterisation of a diode. For the purpose of determining current density, the area of the structure (shown in Figure 4.1) depends on the third dimension and here it is given a value of 355 µm to account for the area of the circular electrodes in the experimental sample. This third dimension is known as the Area Factor (AF) in TCAD's 2-D simulation mode. A simple sandwich (*S* = 0) structure was also simulated for comparison. It was established that *S* = 450 µm is a good representation of the diodes based on the *I-V* results (i.e. the variation of the current becomes negligible for *S* beyond 450 µm). Therefore, it was appropriate to undertake the major work of the study with *S* = 450 µm to show the effect of varying the key performance parameters ($q\phi_m$, R_D, and BL).

For 3-D simulation mode, the circular contact diameter is 400 μm (same diameter as the experimental sample). The sliced ⅛ section of the diode has a right angled triangular surface area with two equal sides of 333.75 μm. An Area Factor of 8 was defined in the 3-D simulation mode to account for the full diode geometry.

A finite element mesh with fine mesh elements located across and near the metal-semiconductor interface was defined for the structure. A number of simulations with variable mesh densities were conducted to determine an appropriate mesh density (minimising simulation time but not compromising on accuracy). A static mesh with an average of 5000 elements for 2-D and one with 800000 elements for 3-D were found to be sufficient to achieve convergence in numerical calculations.

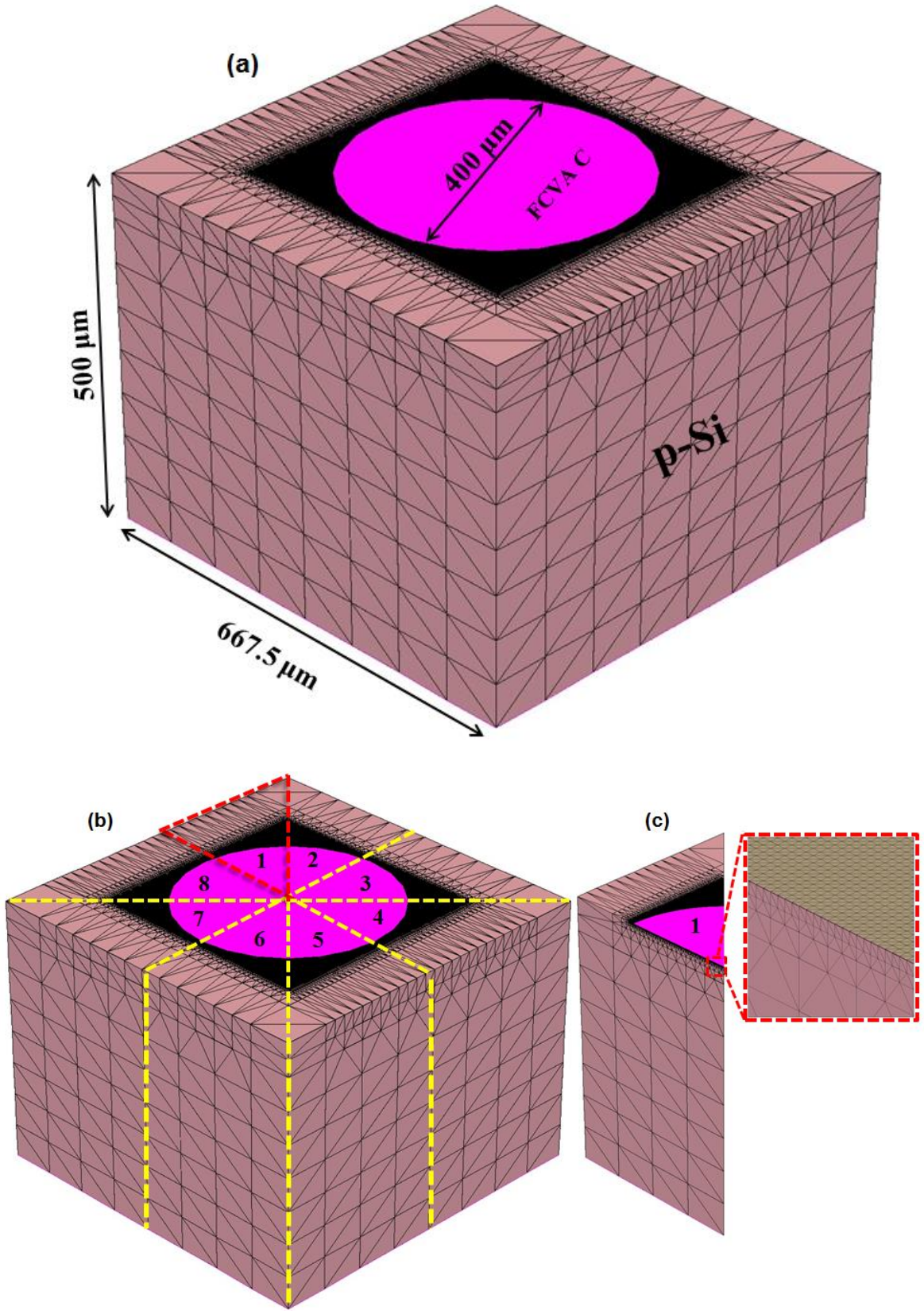

Figure 4.2: (a) Full structure of 3-D M-R-S diode generated in Sentaurus TCAD showing the details of geometry, materials, and contacts. (b) An illustration showing the slicing procedure and (c) the simulated ⅛ section and its meshing details.

4.3 Numerical Device Physics and Boundary Conditions

Assuming Fermi statistics, the SDEVICE default Drift-Diffusion (D-D) model was utilised to simulate the carrier transport in the devices. The *OldSlotBoom* model was applied to model the bandgap structure of p-Si and bandgap narrowing effects. This simulation framework (described in detail in subsection 2.3.2) was used in the SDEVICE TCAD tool for all the M-R-S diode structure simulations. The SDEVICE's physics models adopted for this study can be classified as:

I. Global device physics models (e.g. carrier statistics, carrier transport model, bandgap structure, and mobility) which are valid for the whole device.
II. MS interface-specific physics models (e.g. Schottky interface model, barrier lowering model, distributed contact resistance model) which are only valid at the MS interface.

4.3.1 Mobility

In SDEVICE, a wide range of mobility models are provided for the user to activate. Appropriate selection from Sentaurus TCAD's built-in mobility models were used to account for the effects of both the interfacial layer and the varying microstructure of the carbon films. For M-R-S simulations, *Masetti*'s [51] and *Canali*'s [52] mobility models were activated. The former model accounts for carrier scattering due to charged impurities which in turn reduces the mobility of charge carriers and is expressed by:

$$\mu_{dop} = \mu_{min1} e^{\left(-\frac{P_C}{N_{total}}\right)} + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_{total}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_{total}}\right)^{\beta}} \quad (4.1)$$

$$\mu_{const} = \mu_L e^{\left(\frac{T}{300\text{K}}\right)^{-\zeta}} \quad (4.2)$$

where:

N_{total} is the total doping concertation;

μ_{const} is the constant mobility model due to phonon scattering;

μ_L is the mobility caused by bulk phonon scattering; and

μ_{min1}, μ_{min2}, and μ_1 are reference mobilities, P_C, C_r, and C_s are reference doping concentrations, α, β, and ζ are exponents. The values and units for each parameter that corresponds to silicon are presented in Table 4.1.

Table 4.1: *Masetti*'s mobility model parameters for silicon at *T*=300K [25].

Parameter	Default value for electrons	Default value for holes	Unit
μ_L	1417	470.5	cm^2/Vs
μ_{min1}	52.2	44.9	cm^2/Vs
μ_{min2}	52.2	0	cm^2/Vs
μ_1	43.4	29.0	cm^2/Vs
P_C	0	9.23×10^{16}	cm^{-3}
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.43×10^{20}	6.10×10^{20}	cm^{-3}
α	0.680	0.719	1
β	2.0	2.0	1
ζ	2.5	2.2	1

Canali's model on the other hand takes into account the saturation of carrier velocity in high electric field regions. The electric field reaches its maximum value at the interface of a Schottky diode. The final mobility is a function of activated low-field mobility (μ_{dop}) and a driving force F_{hfs}:

$$\mu(F) = \frac{(\alpha_1+1)\mu_{dop}}{\alpha_1+\left[1+\left(\frac{(\alpha_1+1)\mu_{dop}F_{hfs}}{v_{sat}}\right)^{\beta_1}\right]^{1/\beta_1}} \tag{4.3}$$

$$\beta_1 = \beta_0\left(\frac{T}{300\text{K}}\right)^{\beta_{exp}} \tag{4.4}$$

$$v_{sat} = v_{sat,0}\left(\frac{T}{300\text{K}}\right)^{v_{sat,exp}} \tag{4.5}$$

$$F_{hfs,n} = |\nabla\psi_n| \qquad F_{hfs,p} = |\nabla\psi_p| \tag{4.6}$$

whrere:

μ_{dop} is doping-dependent mobility (i.e. calculated by substituting the parameters from Table 4.1 into eqs. (4.2) and (4.1));

F_{hfs} is the driving force (or field) for charge carriers (i.e. $F_{hfs,n}$ for electrons and $F_{hfs,p}$ for holes);

v_{sat} is the saturation velocity ;

β_1 is a temperature-dependent exponent; and

α_1, β_0, β_{exp}, $v_{sat,0}$, and $v_{sat,exp}$ are model parameters with values listed in Table 4.2.

Table 4.2: *Canali*'s mobility model parameters for silicon at *T*=300K [25].

Parameter	Default value for electrons	Default value for holes	Unit
α_1	0	0	1
β_0	1.109	1,213	1
β_{exp}	0.66	0.17	1
$v_{sat,0}$	1.07×10^7	8.37×10^6	cm/s
$v_{sat,exp}$	0.87	0.52	1

Both mobility models are temperature dependent and a temperature of 300 K was assumed in all of the simulation work.

4.3.2 MS interface-specific physics models

In this subsection, attention will be devoted to the crucial part of the M-R-S approach (i.e. simulation of the interfacial layer). To model the effects of this layer, a Schottky interface between the p-Si substrate and the metal contact (i.e. graphitic carbon) was defined in the SDEVICE command file.

A. Schottky boundary conditions

When a Schottky interface is defined between a semiconductor region and metal region, a set of boundary conditions are placed to simulate the rectification behaviour observed in MS Schottky interfaces. The boundary conditions can be written as [25]:

$$\psi = \psi_F - \phi_B + \frac{kT}{q} ln\left(\frac{N_C}{n_{i,eff}}\right) \qquad (4.7)$$

$$\overrightarrow{J_n}.\hat{n} = qv_n(n - n_o^B) \quad \overrightarrow{J_p}.\hat{n} = -qv_p(p - p_o^B) \qquad (4.8)$$

$$n_o^B = N_C e^{\left(\frac{-q\phi_B}{kT}\right)} \quad p_o^B = N_V e^{\left(\frac{-E_{g,eff}-q\phi_B}{kT}\right)} \qquad (4.9)$$

where:

ψ_F [V] is the Fermi potential at the metal contact;

ϕ_B [V] is the barrier height;

$v_n = 2.573 \times 10^6$ [cm/s] and $v_p = 1.93 \times 10^6$ [cm/s] are the thermionic emission velocities (default values in SDEVICE); and

n_o^B and p_o^B are the equilibrium (zero bias) electrons and holes densities, respectively.

Since the parameters for modelling the bandgap structure of silicon remain unchanged for this study (Table 2.1), the value of the barrier height ϕ_B in eq. (4.7) is mainly affected by the value of the effective metal work function $q\phi_m$. Another important parameter in eq. (4.7) is ψ_F which equals to the applied bias V_A if no resistive effects are considered. For the M-R-S diode structure, resistive effects observed in the fabricated diodes are accounted for at the interface and are numerically represented by a distributed contact resistance model. Consequently, a distributed voltage drop boundary condition is added to the aforementioned boundary conditions (eq. 4.7 to eq.4.9) such that:

$$\Delta\psi(R_D) = R_D(\vec{J}_n + \vec{J}_p + \vec{J}_D).\hat{n} \qquad (4.10)$$

where $\Delta\psi(R_D)$ is the voltage drop across the MS interface and R_D is the distributed contact resistance at the interface.

B. Distributed contact resistance (R_D) model

In a resistive Schottky contact, the Fermi potential ϕ_F at the surface of the semiconductor is no longer equal to the applied voltage V_A. The resistive effects can be emulated by assigning an appropriately scaled resistance R_i to each boundary node *i* with an associated contact length d_i at the MS interface as shown in Figure 4.3. Thus, unlike the lumped resistance model where ϕ_F is constant everywhere in the contact, an electrostatic potential (or Fermi potential) ϕ_{Fi} is associated with each node *i* within the MS interface [25]. Incorporating this model in the simulation will lead to an even distribution of the current throughout the interface which is considered more practical [53].

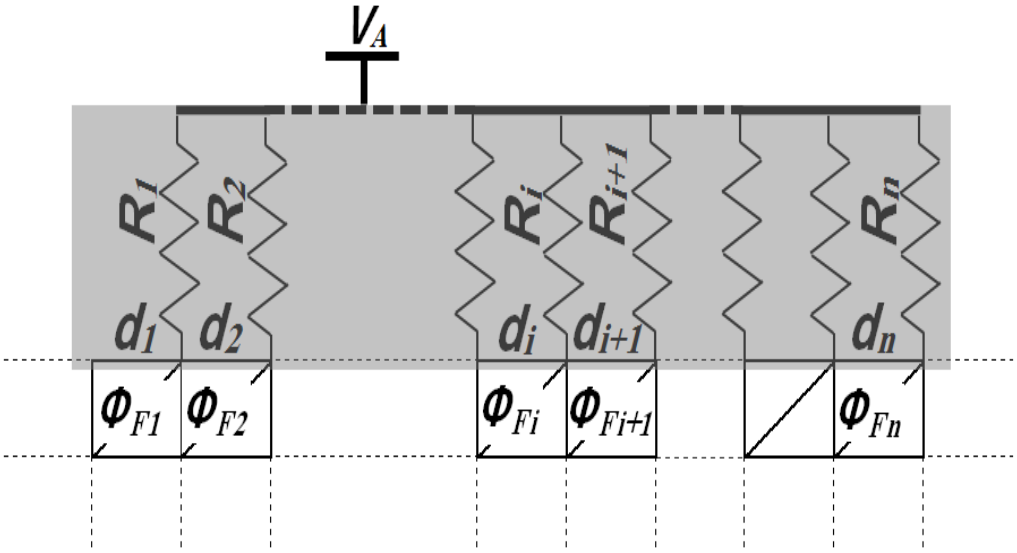

Figure 4.3: Schematic representation of the distributed contact resistance model where d_i is the dimension of each mesh element at the interface. A few elements at the 'top' of the mesh are shown. R_i (determined by R_D and the mesh element dimensions) is the finite resistance at node i, V_A is the applied voltage, ϕ_{Fi} is the Fermi potential at node i, R_D (an input parameter) is the resultant distributed contact resistance, and n is the total number of nodes at the metal semiconductor interface. (The schematic shows the triangular elements used in the generated mesh in Figure 4.2 (c)).

The value of the resultant distributed contact resistance R_D has been iteratively calibrated in order to achieve the best *I-V* curve fit (in forward bias) for the diodes. Curve fitting works in this situation because there is only one parameter (R_D) to vary at this stage and the result is a unique value of R_D. The effective metal work function $q\phi_m$ is determined independently.

C. Schottky Barrier Lowering (BL) model

For the reverse bias characteristics, I_s does not saturate as anticipated by the ideal theory [6]. It rather increases as the applied reverse bias voltage increases. This is because the value of the barrier height ϕ_B is not bias-independent as the theory assumes but instead, it decreases slightly as the applied bias increases [6]. Due to the exponential dependency of I_s on ϕ_B, a slight decrease of ϕ_B has a

significant effect on the magnitude of I_s. For this work, the Barrier Lowering (BL) model has been activated at the MS interface to account for this effect. Image force is the most important physical mechanism accounted for in the model and the amount by which the barrier is lowered denoted $\Delta\phi_B$, depends entirely on the applied electric field [25]:

$$\Delta\phi_B(F) = \begin{cases} a_1\left[\left(\frac{F}{F_o}\right)^{p_1} - \left(\frac{F_{eq}}{F_o}\right)^{p_{1,eq}}\right] + a_2\left[\left(\frac{F}{F_o}\right)^{p_2} - \left(\frac{F_{eq}}{F_o}\right)^{p_{2,eq}}\right] & \text{if } F > \eta F_{eq} \\ 0 & \text{if } F \le \eta F_{eq} \end{cases} \quad (4.11)$$

where:

$F_o = 1$ [V/cm] is the model parameter electric field (default value);

η=1 (default value);

F_{eq} is the value of electric field at equilibrium; and

$a_1 = 2.6 \times 10^{-4}[e\text{V}], p_1 = p_{1,eq} = 0.5,\ a_2 = 0\ [e\text{V}]$, and $p_2 = p_{2,eq} = 1$

are coefficients with default values for eq. (4.11).

Barrier lowering has been observed in our devices and in similar carbon/Si devices by other authors in recent experimental works [54, 55]. The authors attributed this characteristic to image force effects [6].

4.4 The algorithm (iterative method)

The study was initiated by conducting 2-D simulations. The 2-D simulation results were then verified by comparing them to the 3-D simulation results and the accuracy in simulating the carbon/p-Si diodes' electrical characteristics in 2-D was established. The *I-V* characteristics were determined by simulating for bias voltages

between -1.0 V to 1.0 V. The algorithm (iterative method) used to simulate the *I-V* characteristics for the M-R-S diode structure is described as follows:

1) $R_D = 0.0\ \Omega\ \text{cm}^2$ and BL model is deactivated.

2) (a) Vary $q\phi_m$ in the range of 4.40 eV to 5.40 eV covering the range of reported values of graphite in literature [56, 57] to generate a set of *I-V* curves.
   (b) $q\phi_m$ range reduced based on results of step 2(a). In this work, the reduced range is from 4.40 eV to 4.60 eV to closely agree with experimental results.

3) (a) Vary R_D for each value of $q\phi_m$ in the reduced range to generate a new set of *I-V* curves.
   (b) R_D range reduced based on results of step 3(a). In this work, the reduced range is from 0.00 to 0.10 $\Omega\ \text{cm}^2$ resulting in closer agreement with experimental results.

4) Activate BL model and compare with experimental *I-V* measurements.

After thoroughly examining the comparison between simulated and experimental *I-V* results, a set of values for both the work function $q\phi_m$ and the distributed contact resistance R_D were targeted to scan for the best fit. In order to achieve excellent agreement in the reverse *I-V* region between simulation and experimental *I-V* results, the BL model has to be activated.

The experimental *I-V* curves and correlating 2-D and 3-D M-R-S diode structure *I-V* curves for the carbon/p-Si diode will be presented in Chapter 5.

Simulation results to study the effect of varying $q\phi_m$ and R_D on the M-R-S Diode's *I-V* characteristics are then presented. Also included are 2-D equipotential plots showing the variation of the electrostatic potential across the silicon substrate for different device geometries when the diode is turned ON. In addition, 3-D maps showing the variation of the electrostatic potential and total current density across a ⅛ section of the full diode structure when the diode is turned ON are presented.

5 Results and Discussion

The chapter begins by reporting and discussing the electrical characterisation results for selected samples obtained using I-V, C-V, and Hall measurements described in chapter 3. In addition, the findings of the Metal-Insulator-Semiconductor (M-I-S) and Metal-Resistor-Semiconductor (M-R-S) TCAD simulations are presented in this chapter with a detailed discussion of the results.

5.1 Experimental Measurements Results

The measured dark *I-V* characteristics of C/p-Si and Pt/p-Si Schottky diodes under forward and reverse bias conditions at room temperature are shown in Figures 5.1 and 5.2, respectively. The *I-V* curves for all diodes show strong rectifying characteristics with linearity under low forward bias conditions ≤ 0.2-to-0.3 V and current saturation under reverse bias. Figure 5.1 reveals that C/p-Si diodes formed at -1.0 kV bias during deposition and on Si substrate at 100 °C have the lowest series resistance while the Pt/p-Si diodes have the highest. It can be seen from the three *I-V* curves plotted in Figure 5.2 that the reverse saturation current, I_s, was significantly higher (100 nA) in the Pt/p-Si diodes than either of the C/p-Si diodes.

Assuming thermionic emission transport as the dominant current transport mechanism across the Schottky junction, the value of the ideality factor *n* of all diodes was calculated from the slope of the linear portion of the forward *I-V* curve (see Figure 5.1) and using eq. (2.14). By extrapolating the linear portion of the forward bias *I-V* curve (see Figure 5.1), the value of I_s was determined from the y-intercept of the extrapolated line. The value of $q\phi_{Bp(I-V)}$ of the diodes can then be computed using eq. (2.17) found in subsection 2.1.3.

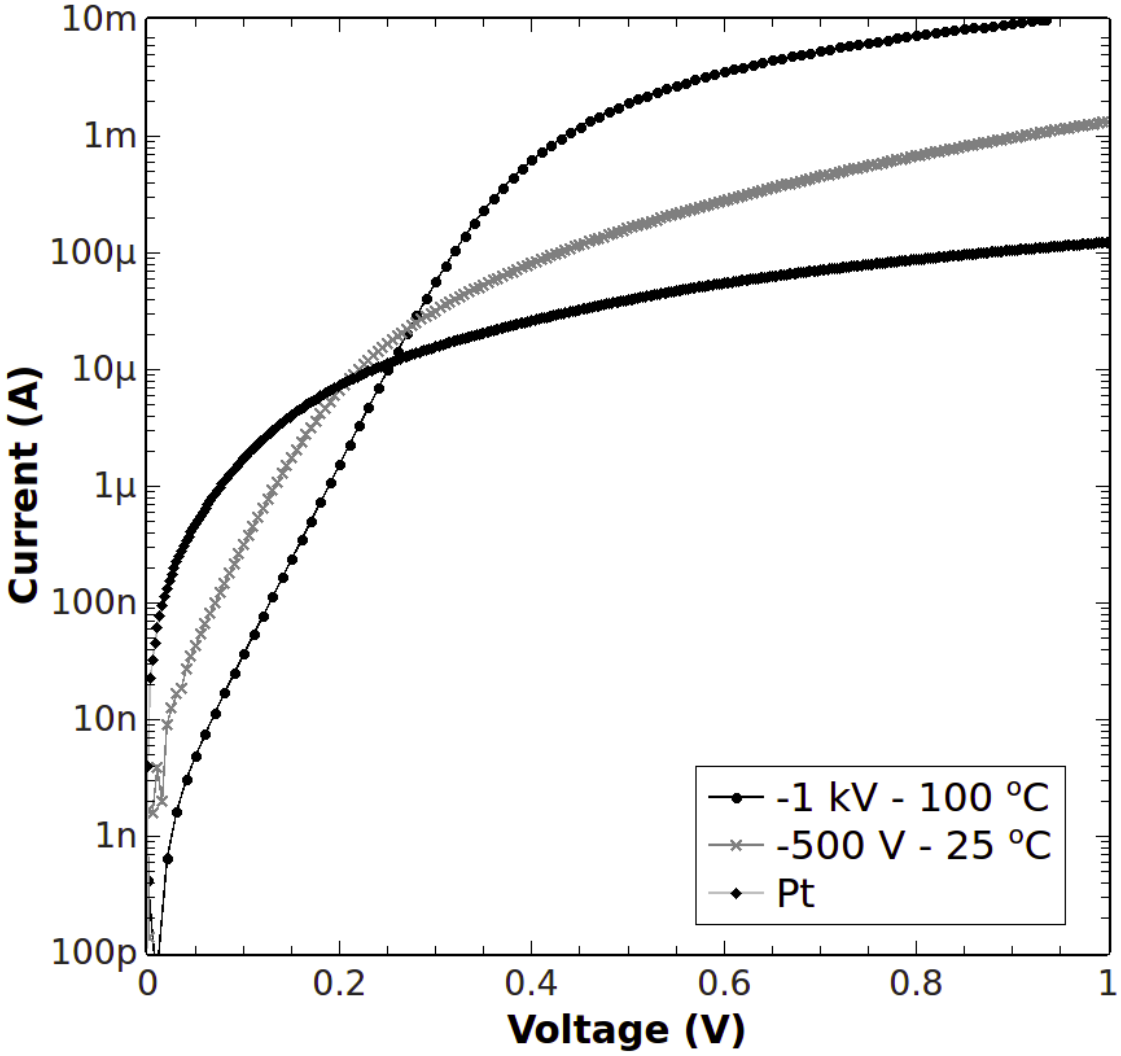

Figure 5.1: Forward *I-V* characteristics of C/p-Si and of Pt/p-Si Schottky diodes measured at room temperature. The C/p-Si diodes were formed at a substrate bias of -1.0 kV and of -500 V and a substrate temperature of 100 °C and of 25 °C, respectively.

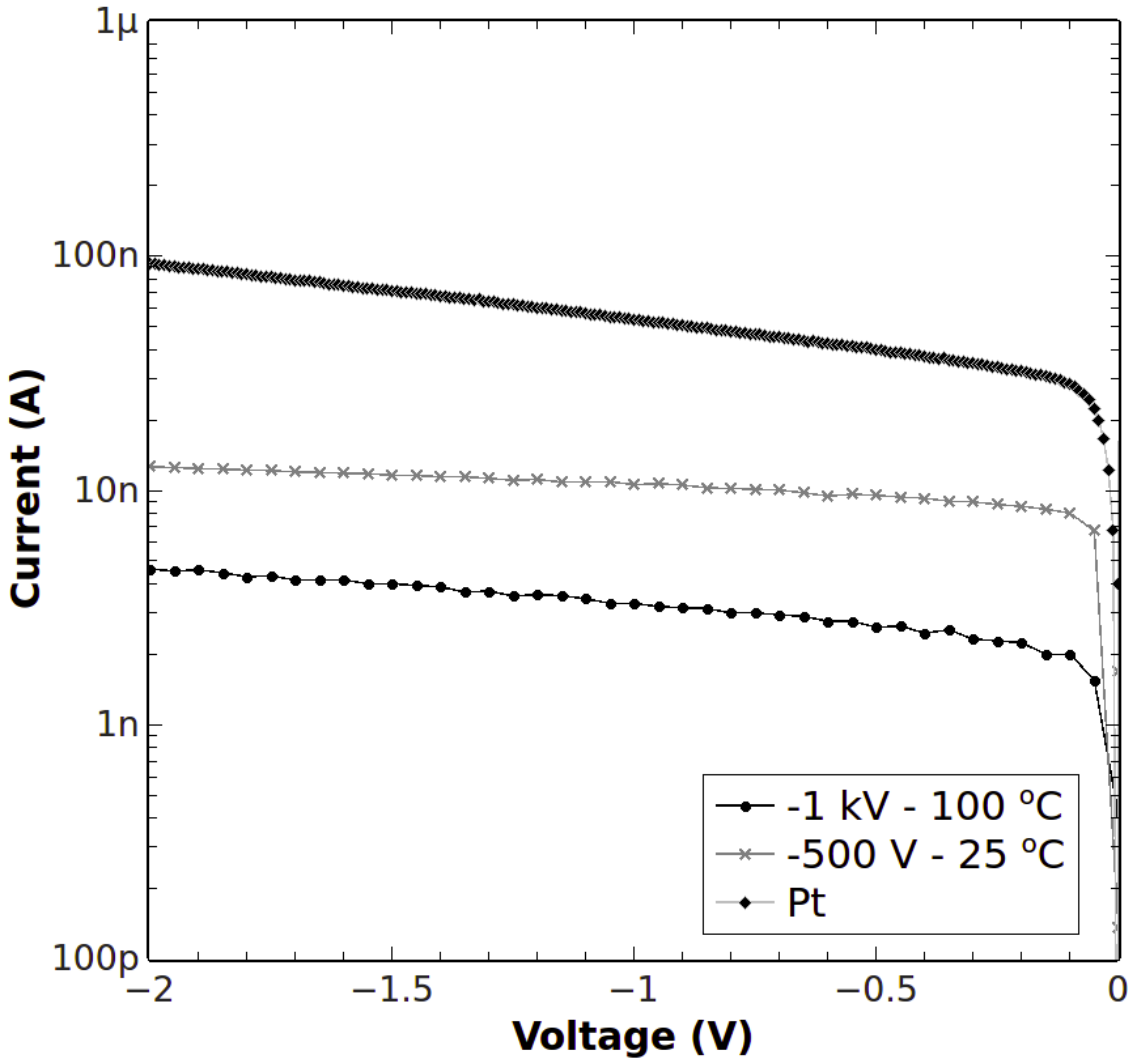

Figure 5.2: Reverse *I-V* characteristics of C/p-Si and of Pt/p-Si Schottky diodes measured at room temperature. The C/p-Si diodes were formed at a substrate bias of -1.0 kV and of -500 V and a substrate temperature of 100 °C and of 25 °C, respectively.

Using capacitance (C) versus voltage (V) measurements, the $1/C^2$ versus V plots of C/p-Si diodes for reverse bias and moderate forward bias are shown in Figure 5.3. These plots are approximately linear indicating a uniform doping concentration (N_A). In addition to *I-V* measurements described above, the value of $q\phi_{Bp\,(C-V)}$ for C/p-Si diodes was calculated using the *C-V* measurements by extrapolating a straight line from the plots to the x-intercept to determine ψ_{bi} and using the following relationship:

$$q\phi_{Bp\,(C-V)} = q\psi_{bi} + q\psi_o + KT \quad (5.1)$$

where ψ_o is defined as the bulk potential of Si based on the effective density of states. Barrier height measurements using the *I-V* method give $q\phi_{Bp(I-V)}$= 0.60 eV for C/p-Si diodes formed at -1.0 kV bias and 100 °C substrate temperature and $q\phi_{Bp(I-V)}$= 0.49 eV for C/p-Si diodes formed at -0.5 kV and 25 °C. For both C/p-Si diodes, typical barrier height values calculated using the *C-V* method (i.e. $q\phi_{Bp(C-V)}$) were higher than values calculated using the *I-V* method (i.e. $q\phi_{Bp(I-V)}$), a finding consistent with the presence of a thin, resistive interface layer.

The rectification ratio (RR) for all diodes was measured as the ratio of the forward and reverse currents at ± 0.9 V. The graphitic carbon diodes formed at -1.0 kV substrate bias and 100 °C substrate temperature exhibited the highest RR of 2.9×10^6 followed by graphitic carbon diodes formed at -0.5 kV and 25 °C. The Pt/p-Si diodes exhibited the lowest RR of 2.1×10^3. In addition to the highest RR, C/p-Si Schottky diodes (deposited at -1.0 kV bias and silicon substrate temperature of 100 °C) exhibited the lowest saturation current (I_s) of 0.02 nA, lowest series resistance (R_s) of 60 Ω, and an ideality factor n = 1.05, making them the best-performing diodes among all fabricated samples. The properties of all diodes, calculated from experimental *I-V* and *C-V* measurements are summarised in Table 5.1.

The values of carrier concentration (N_A) and mobility of p-Si calculated using Hall effect measurements were 8.0×10^{15} cm^{-3} and 450 cm^2/Vs, respectively. The mobility (450 cm^2/Vs) was compared with values in the literature for high quality single crystal p-Si and these compared favourably [6].

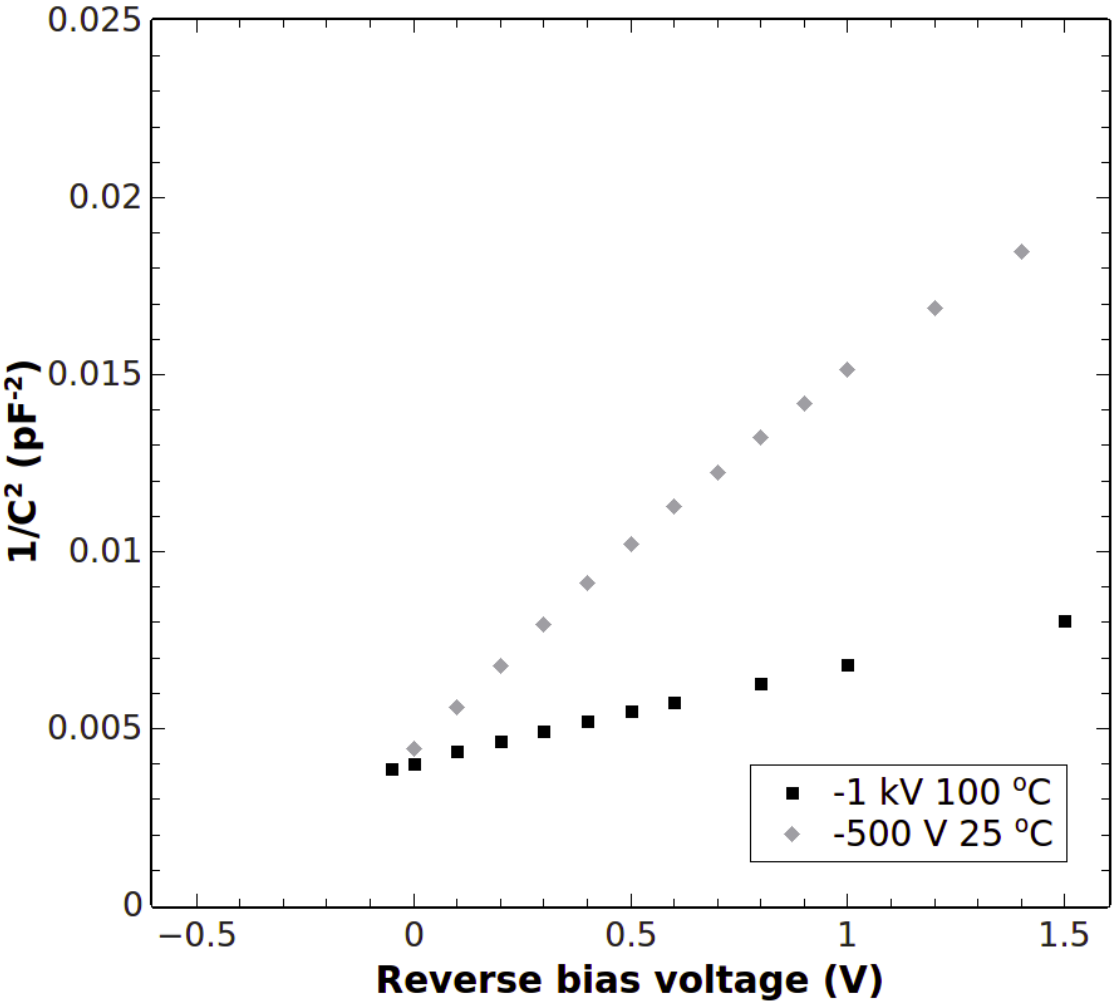

Figure 5.3: Plots of $1/C^2$ versus reverse bias voltage for C/p-Si Schottky diodes. The C/p-Si diodes were formed at a substrate bias of -1.0 kV and of -500 V and a substrate temperature of 100 °C and of 25 °C, respectively.

Figure 5.4 shows an XTEM image for the diode sample (-1 kV, 100 °C). This specimen was prepared using a FEI Scios focussed-ion/electron beam system.

Table 5.1: Electrical characteristics of C/p-Si and Pt/p-Si Schottky diodes. The C/p-Si diodes were formed at a substrate bias of -1.0 kV and of -0.5 kV and a substrate temperature of 100 °C and of 25 °C, respectively.

Diode structure	I_s (nA)	n	RR at ± 0.9 V	R_s (Ω)	$q\phi_{Bp(I-V)}$ (eV)	$q\phi_{Bp(C-V)}$ (eV)
C/p-Si (-0.5 kV, 25 °C)	1.72	1.05	9.2×10^4	600	0.49	0.66
C/p-Si (-1.0 kV, 100 °C)	0.02	1.05	2.9×10^6	60	0.60	1.50
Pt/p-Si	100	1.40	2.1×10^3	1200	0.40	-

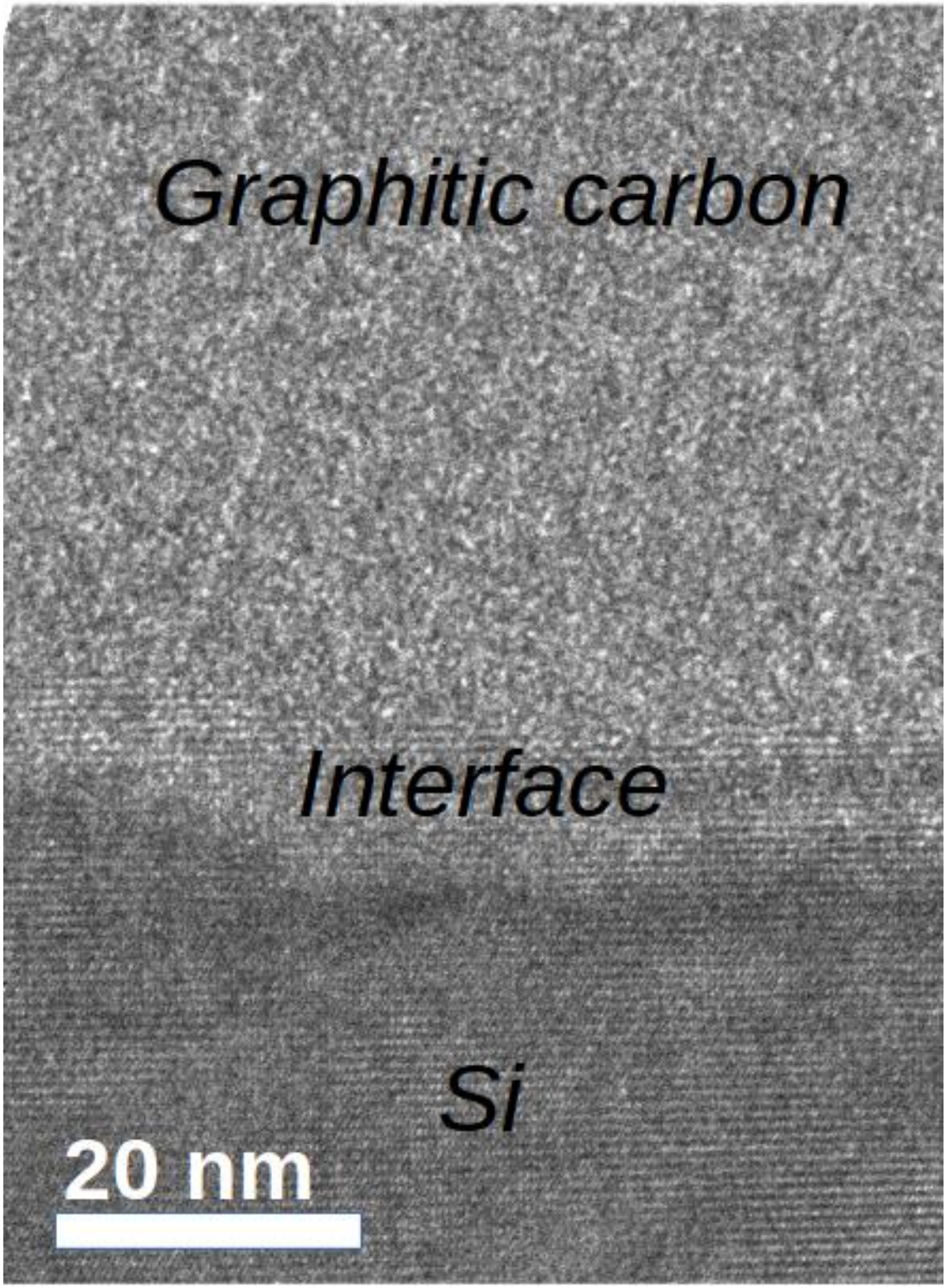

Figure 5.4: An XTEM micrograph of the Schottky junction formed between the graphitic carbon film energetically deposited at -1.0 kV substrate bias and 100 °C substrate temperature and Si.

5.2 Metal-Insulator-Semiconductor (M-I-S) TCAD Simulations Results

Simulated *I-V* characteristics for both C/p-Si diodes formed at -1.0 kV substrate bias and 100 °C substrate temperature (and also at -0.5 kV, 25 °C) based on an M-I-S TCAD structure model with corresponding experimental *I-V* measurements are shown in Figure 5.5.

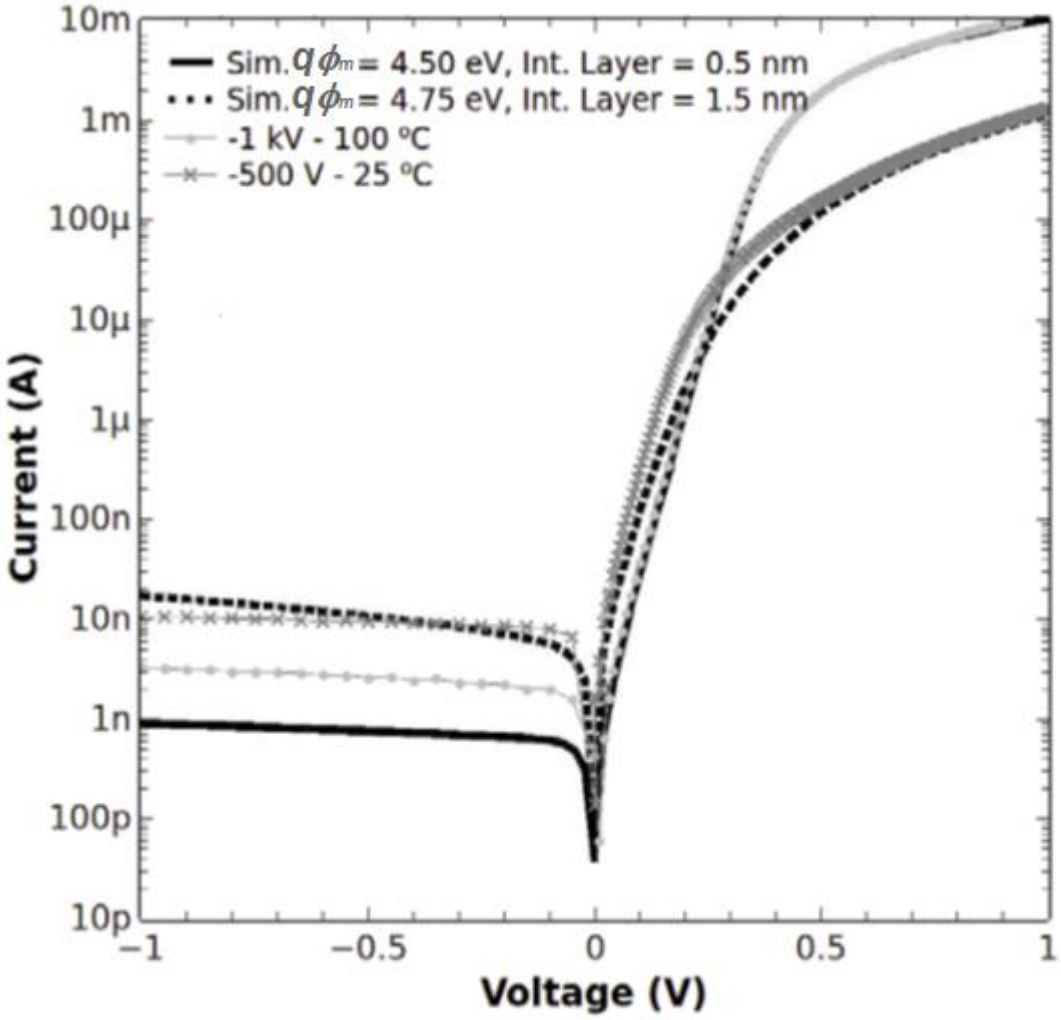

Figure 5.5: Current-Voltage plots for the M-I-S model diode structures generated using Sentaurus TCAD with corresponding experimental measurements using a) $q\phi_m$ of 4.50 eV and a native oxide (SiO_2) layer with thickness of 0.5 nm and b) $q\phi_m$ of 4.75 eV and SiO_2 layer with thickness of 1.5 nm.

The best correspondence with the measurements for C/p-Si diode (-1.0 kV, 100 °C) was obtained using a native oxide layer (mainly SiO_2) with a thickness of 0.5 nm and a carbon (the metal in the MIS model) workfunction $q\phi_m$ of 4.50 eV. For the C/p-Si diode (-0.5 kV, 25 °C), an oxide thickness of 1.5 nm and $q\phi_m$ of 4.57 eV resulted in the best correspondence with experimental *I-V* measurements.

5.3 M-R-S TCAD Simulations Results

The best fits in 2-D and 3–D for the best-performing C/p-Si diodes (formed at -1.0 kV and 100 °C substrate conditions) with corresponding experimental *I-V* measurements are shown in Figure 5.6. The simulated *I-V* characteristics presented in Figure 5.6 are based on the structure shown in Figure 4.1 with S = 450 μm for 2-D simulation mode and ⅛ section shown in Figure 4.2 (c) for the 3-D mode. (Because of 3D symmetry, a model of only ⅛ of the whole diode is required for simulating the electrical behaviour as the results are mirrored in every other ⅛ section).

The corresponding values of $q\phi_m$ and R_D used to obtain excellent agreement for the best fits are summarised in Table 5.2. Excellent agreement is observed between the 2-D and 3-D simulated M-R-S structures and the experimental *I-V* measurement results. It was found that the 2-D approach is ~1000 faster than the 3-D approach making it more time-efficient for performing long iterative simulations and very useful when time and/or computational resources are limited.

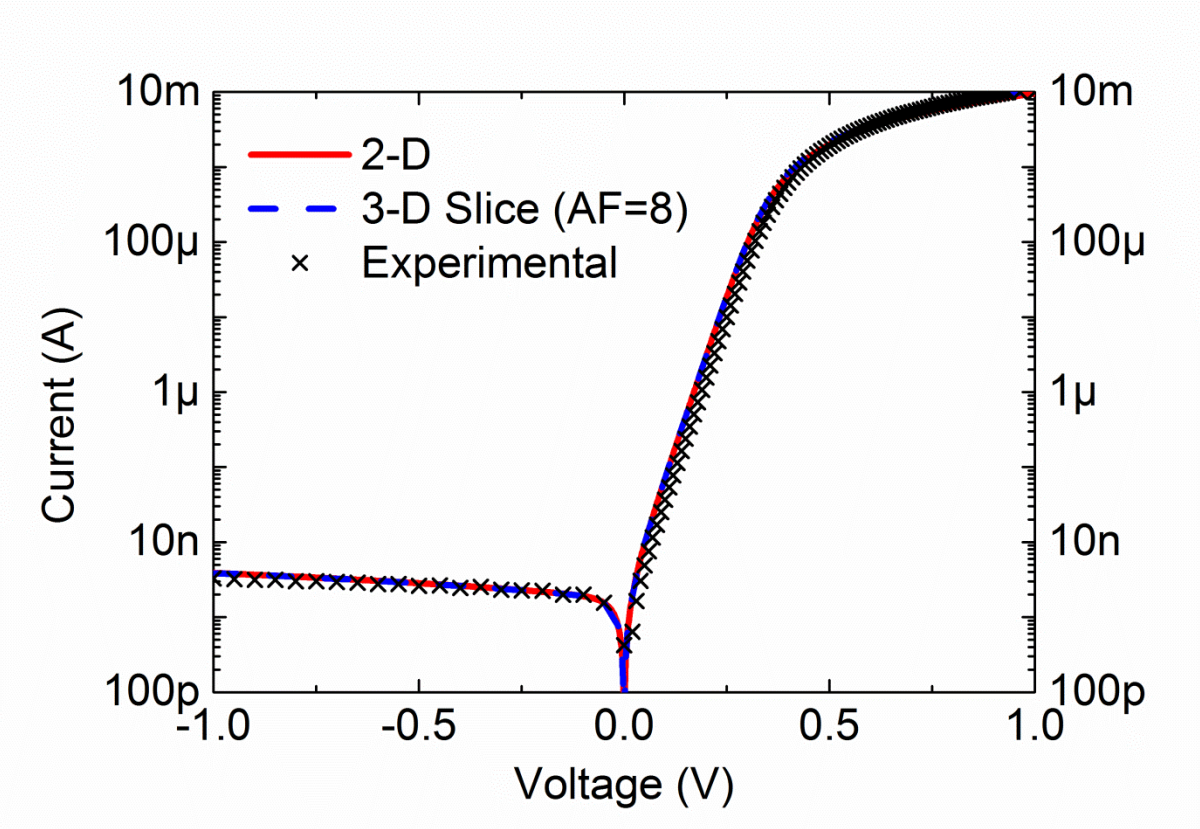

Figure 5.6: Current-Voltage plots for the 2-D and 3-D M-R-S diode structures generated using Sentaurus TCAD with best fit parameters for comparison with experimental results of C/p-Si (-1.0 kV, 100 °C) diodes. For the 3-D simulation result, AF (a TCAD term) is the Area Factor = 8 to account for the full diode structure. The model parameters are listed in Table 5.2.

In order to achieve excellent agreement in the reverse *I-V* region between the simulated M-R-S 2-D or 3-D structures and experimental *I-V* measurements, the BL model must be activated. The activation of the (Barrier Lowering) BL model resulted in the adjustment of I_s along the reverse bias region of the curve to match the experimental *I-V* measurements. As can be seen from Figure 5.7, activation of this model affects the simulated *I-V* characteristics in the reverse bias range.

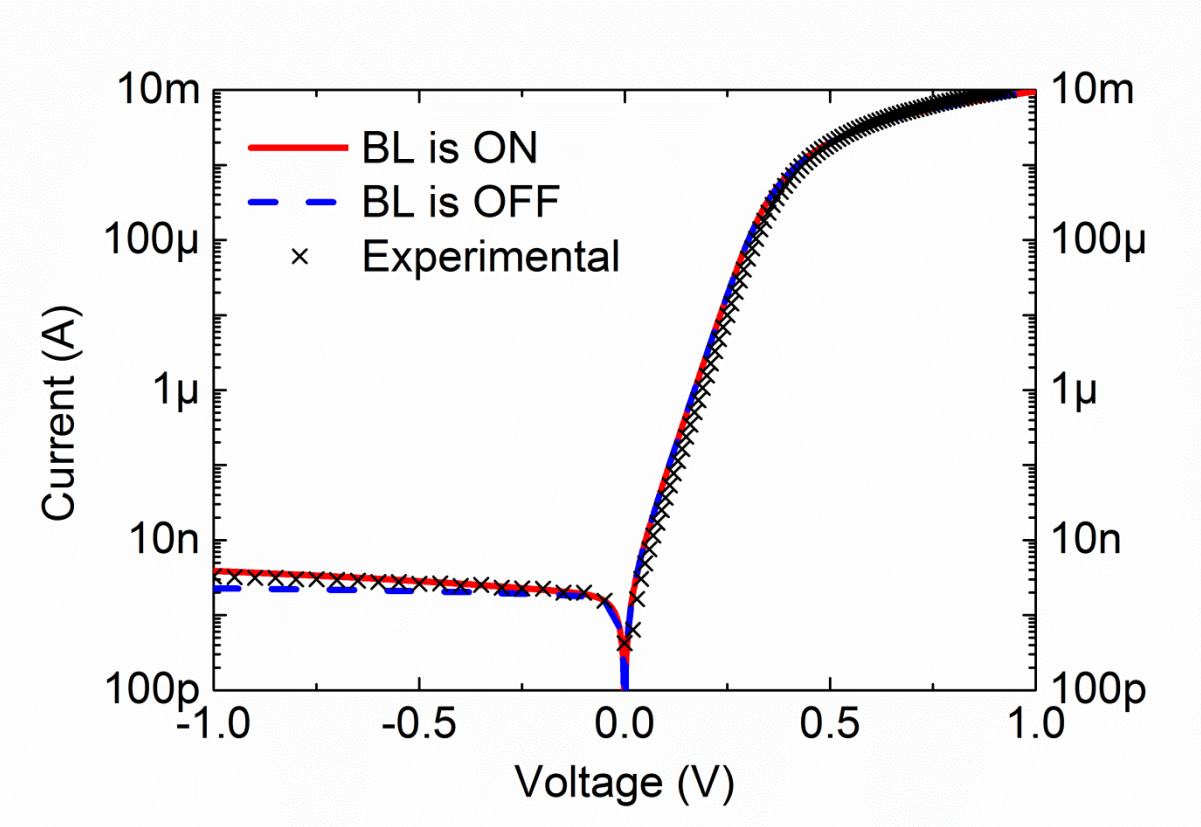

Figure 5.7: Current-Voltage plots for the M-R-S diode structure generated using Sentaurus TCAD with and without activating the (Barrier Lowering) BL model with best fit parameters for comparison with experimental results of C/p-Si (-1.0 kV, 100 °C) diodes. The model parameters are listed in Table 5.2.

For 2-D simulations, the effect of varying *S* on the diode's *I-V* characteristics and on electrostatic potential contour plots within the structure have been studied as illustrated in Figure 5.8 and Figure 5.9, respectively. From the *I-V* characteristics shown in Figure 5.8 it can be established that there are no obvious effects appearing from extending *S* beyond 450 µm for either the forward or reverse currents characteristics of the diode within the simulated bias range (- 1.0 V≤ V ≤ 1.0 V).

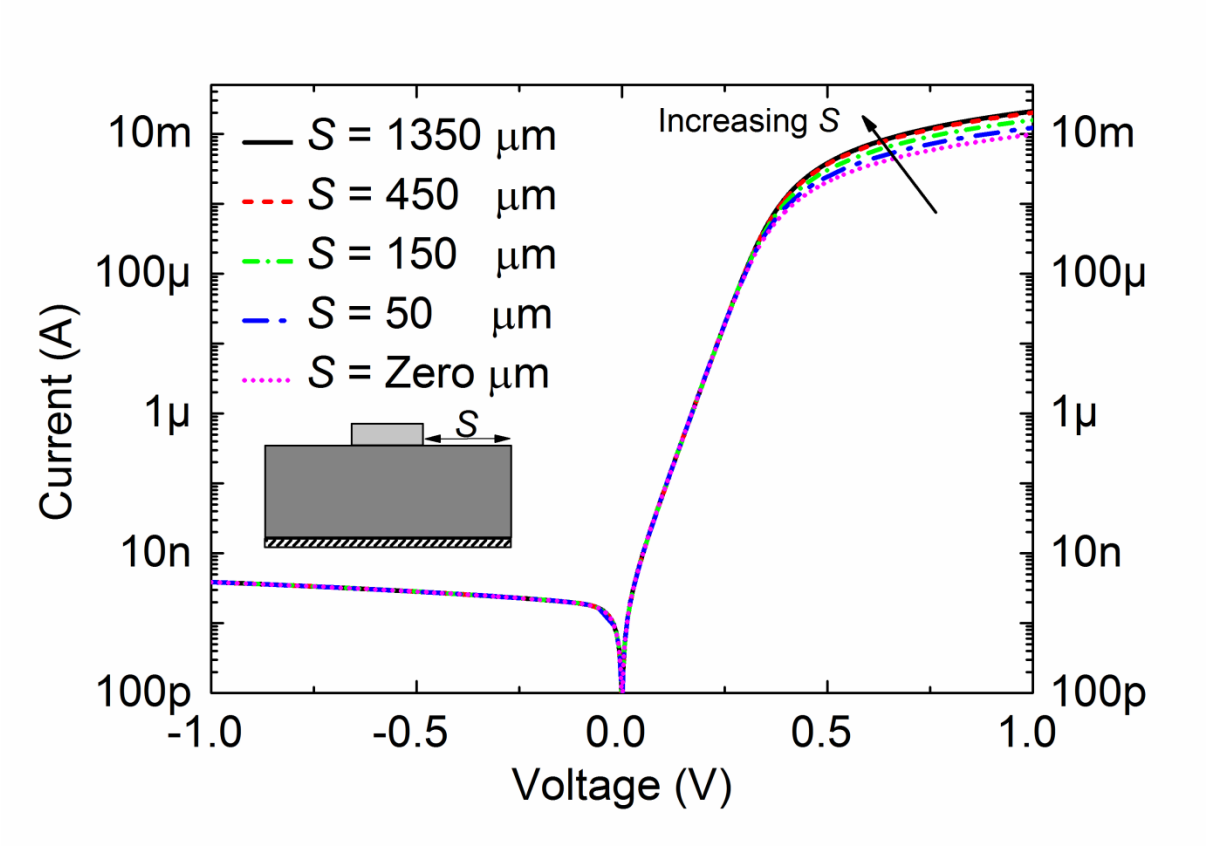

Figure 5.8: Current-Voltage plots for the 2-D M-R-S diode structure generated using Sentaurus TCAD showing the effect of varying *S*. (The inset shows the relative dimension of the Schottky (top) and the ohmic contacts (bottom)). The model parameters are listed in Table 5.2.

In addition to the *I-V* plots in Figure 5.8, the insets in parts (c) and (d) in the 2-D electrostatic potential contour plots shown in Figure 5.9 confirm that diodes with *S* = 450 µm are equivalent to *S* =1350 µm electrically because they both have equivalent electrostatic potential distribution in the silicon region surrounding the contact region. Therefore, based on these results, experimental diodes (with infinite *S*) can be accurately represented using 2-D models with *S*= 450 µm. The electrostatic potential of the same diode was also simulated in 3-D (see Figure 5.10 (a)) using the structure shown in Figure 4.2 (c). Also, 3-D contour maps showing the variation of the total current density for the same structure is presented in Figure 5.10 (b).

The effect of varying $q\phi_m$ ('metal' work function) on the *I-V* curve is shown in Figure 5.11. It is very apparent that the reverse saturation current is very sensitive to small changes in the value of $q\phi_m$. A minor increase in $q\phi_m$ caused significant deterioration in the diode's reverse saturation current (from A to B in Figure 5.11) and consequently a substantial (four orders of magnitude) drop in the RR of the simulated diodes occurred. The same can be said for the forward current; however, it can be noted that its sensitivity gradually vanishes as bias voltage increases especially after V= ~ 0.75 V. The sensitivity of reverse saturation current to the work function suggests that the model can provide an accurate estimate of the work function in the experimental devices. This modelling outcome is extremely valuable because determining the value of the work function at the interface is not possible experimentally. The model predicts a significant increase in the simulated rectification ratio if the work function is reduced. This suggests a route to improve these devices.

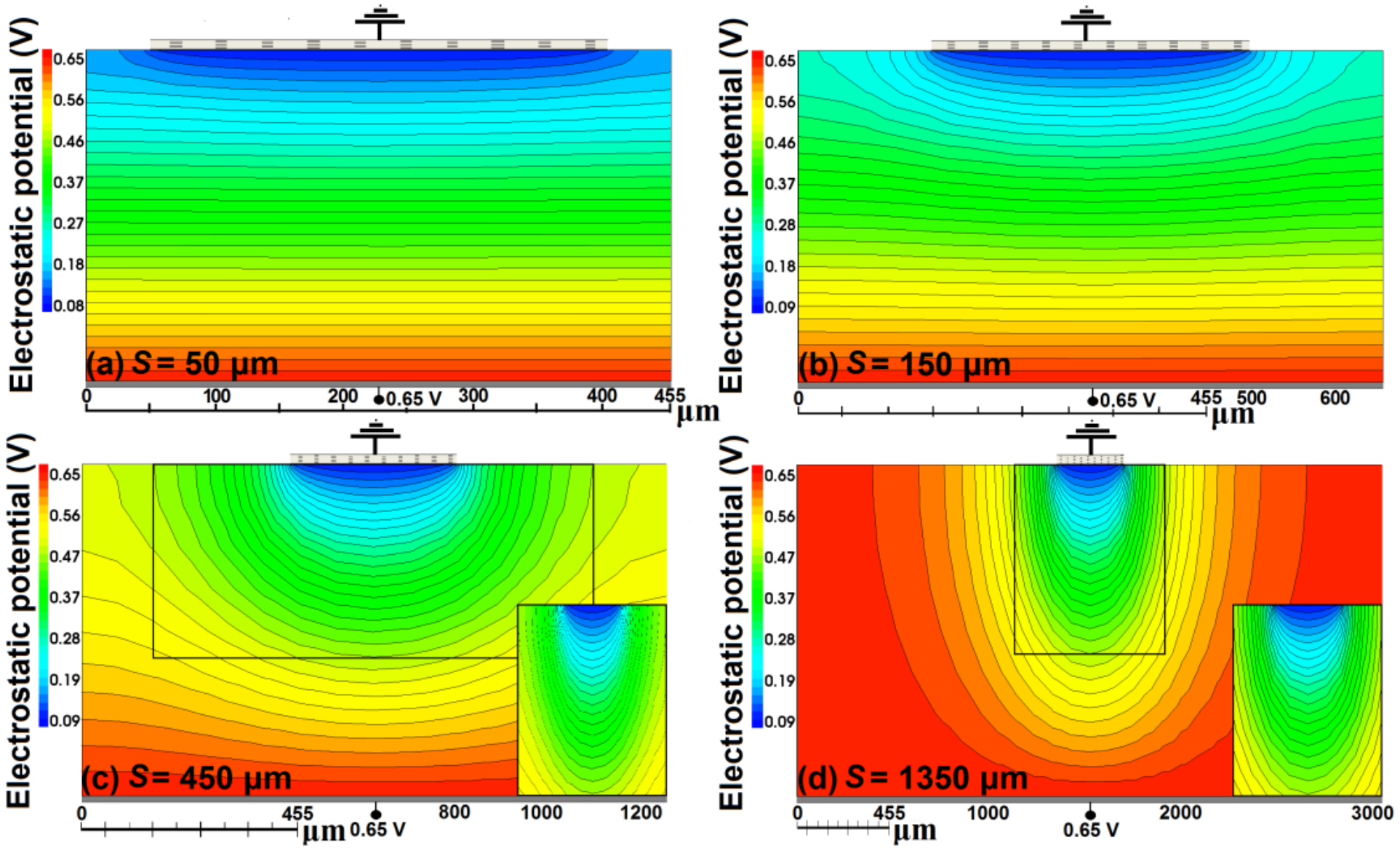

Figure 5.9: Simulation results for electrostatic potential variation across the Si substrate at forward bias of 0.65 V for the 2-D M-R-S diode structure generated using Sentaurus TCAD for (a) *S* =50 µm, (b) *S* =150 µm, (c) *S* =450 µm, and (d) *S* =1350 µm. The model parameters are listed in Table 5.2.

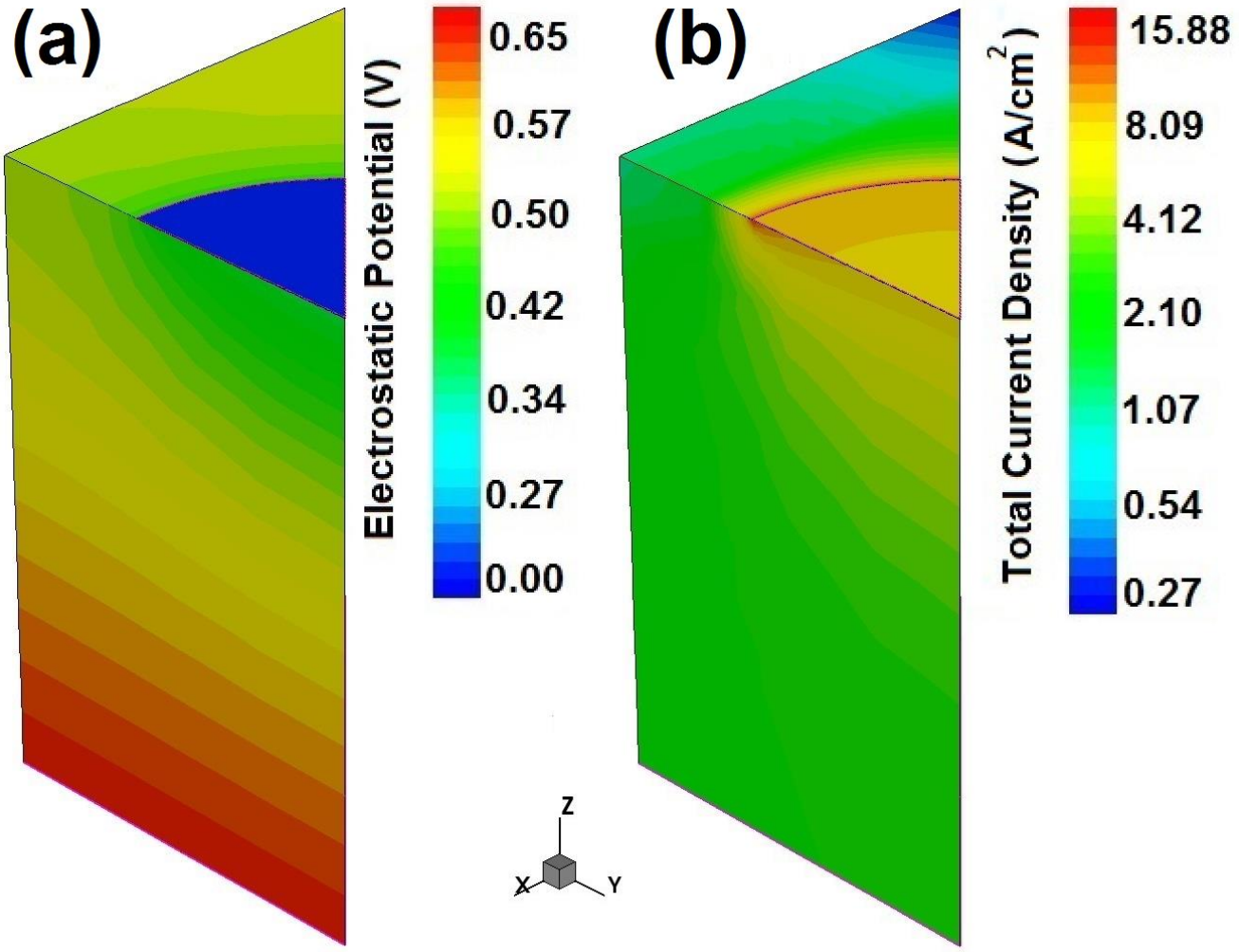

Figure 5.10: 3-D output maps showing the variation of (a) the electrostatic potential and (b) the total current density at forward bias of 0.65 V for the 3-D M-R-S diode structure generated using Sentaurus TCAD.

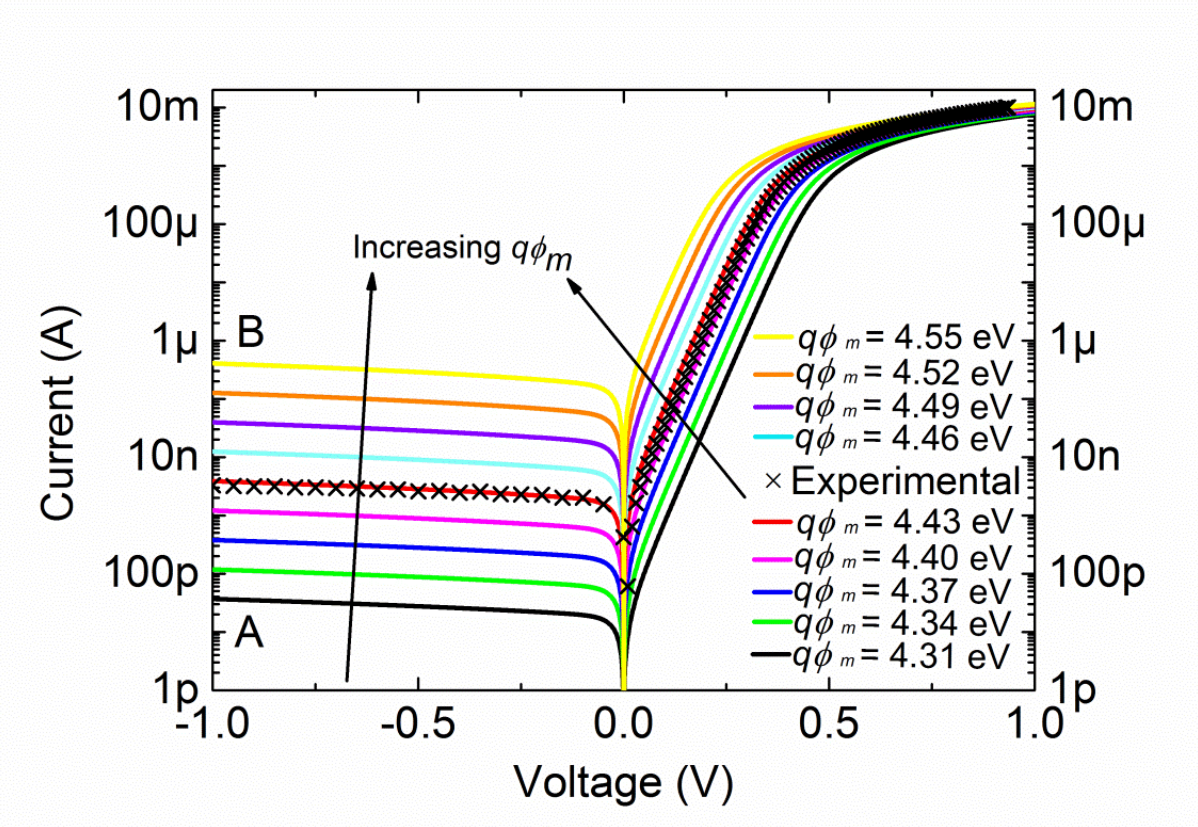

Figure 5.11: Current-Voltage plots for the M-R-S diode structure generated using Sentaurus TCAD with experimental results of C/p-Si (-1.0 kV, 100 °C) diodes showing the effect of varying $q\phi_m$ (from A to B) with best fit parameters. R_D = 0.04 Ω cm^2 and S = 450 µm.

Figure 5.12 shows the effect of varying R_D in the M-R-S structure model. This parameter has no effect on the reverse bias current (unlike $q\phi_m$) and the forward bias current is not sensitive to small changes in R_D. The plots show that an R_D value of 0.04 Ω cm^2 provides good agreement with the experimental data. Incorporating this value has a pronounced effect on the *I-V* characteristics of the junction model for the forward bias region ≥ 0.5 V, when compared with a junction with no interface resistance. This resistance is attributed to the carbon/Si mixed interfacial layer of ~3 nm thickness, as observed by XTEM.

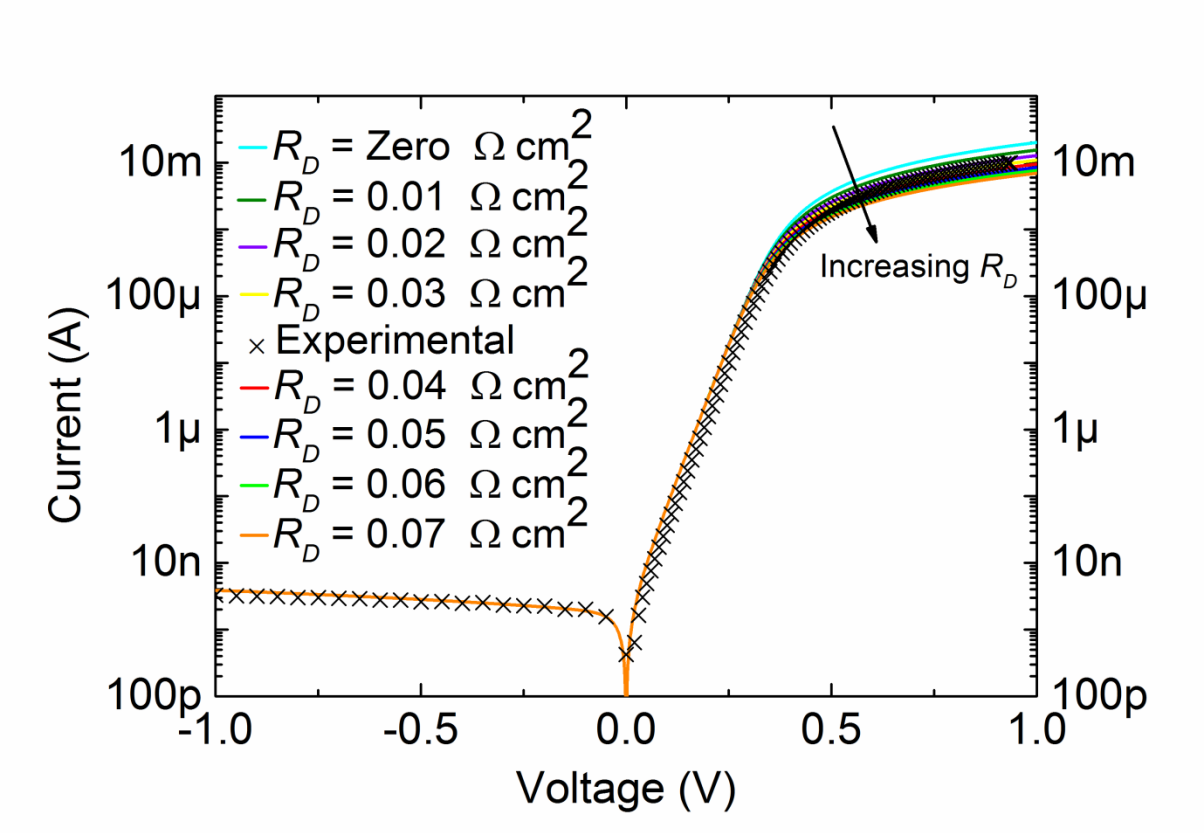

Figure 5.12: Current-Voltage plots for the M-R-S diode structure generated using Sentaurus TCAD with experimental results of C/p-Si (-1.0 kV, 100 °C) diodes showing the effect of varying R_D with best fit parameters. $q\phi_m$= 4.43 eV and S = 450 µm.

The best fit in 2-D for C/p-Si diodes (formed at -0.5 kV and 25 °C) with corresponding experimental *I-V* measurements are shown in Figure 5.13. The simulated *I-V* characteristics presented in Figure 5.13 are based on the structure shown in Figure 4.1 with S = 450 µm for 2-D simulation mode. A reduction in the quality of agreement between the model and experimental data is observed in the forward bias region 0.3 V ≤ V ≤ 0.7 V. In order to simulate the observed RR at ± 1 V, the values of $q\phi_m$ and R_D has to be increased to reach 4.47 eV and 0.74 Ω cm^2 in the M-R-S model, respectively. Nevertheless, the experimental *I-V* plots in Figure 5.13 show lower values of current compared to the M-R-S model within this region. This indicates that a different resistive effect that only targets the current within this region

needs to be added on top of the interface resistance R_D to improve the agreement with experimental data which ultimately demonstrates that carbon films deposited at lower bias (i.e. lower deposition energy) forms highly resistive contact due to the reduced sp^2 fraction [15]. This outcome is consistent with recent observations of similarly deposited C/6H-SiC diodes [58].

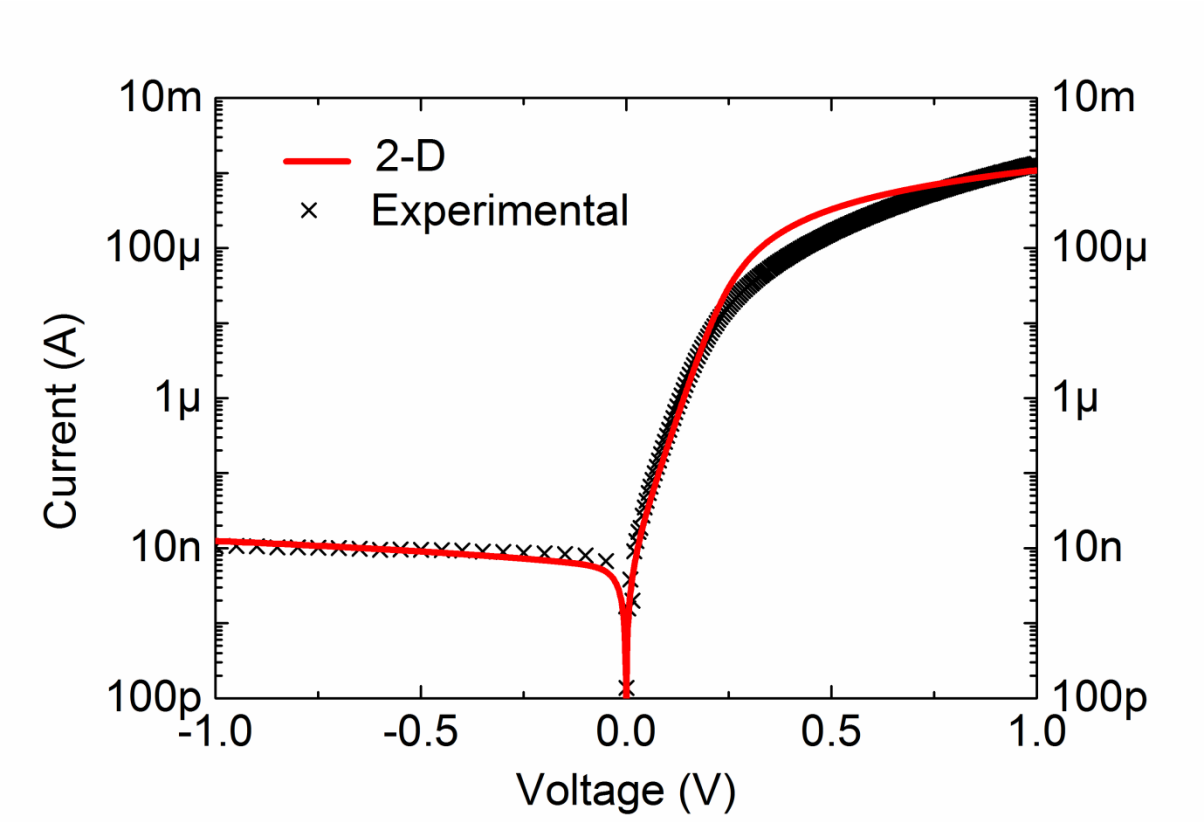

Figure 5.13: Current-Voltage plots for the 2-D M-R-S diode structures generated using Sentaurus TCAD with best fit parameters for comparison with experimental results of C/p-Si (-0.5 kV, 25 °C) diodes. The model parameters are listed in Table 5.2.

Table 5.2: Values of the M-R-S model parameters used to achieve agreement with experimental *I-V* measurements of C/p-Si Schottky diodes.

Diode	$q\phi_m$ (eV)	R_D (Ω cm^2)	BL
C/p-Si (-1.0 kV, 100 °C)	4.43	0.04	ON
C/p-Si (-0.5 kV, 25 °C)	4.46	0.74	ON

6 Conclusions and Future Work

6.1 Conclusions

The fabrication, electrical characterisation, and TCAD simulation of carbon contacts to p-type Si have been investigated in this thesis. Energetically deposited graphitic (semi-metallic) carbon thin films using Filtered Cathodic Vacuum Arc (FCVA) technique onto p-Si substrates formed highly rectifying junctions. The electrical properties of these thin films can be tuned to achieve the desired Schottky diode performance. Applying a substrate bias of – 1.0 kV at a substrate temperature of 100 °C has produced carbon diodes with rectification ratios (RR) exceeding six orders of magnitude, saturation current densities (J_s) in the low nanoamp/cm^2 range, and ideality factors (n) approaching unity.

The extremely low n of 1.05 for these graphitic carbon diodes was lower than recently reported for Schottky diodes based on graphene [9-11] and graphenic carbon [46]. The same can be said for the high RR of ~3×10^6. Unlike C/Si diodes reported in [11, 46], these desirable values were attained without any structural optimisations. Examples of structural optimisations are guard rings (as in ref. 46) and SiO_2 passivation (as in ref. 11, 46). Another important advantage is the relatively low temperature formation/deposition process, making it compatible with standard photolithography which enables precise control of device dimensions/locations. Furthermore, FCVA deposition systems are readily used on an industrial scale thanks to their high growth rates allowing for low capital cost [59]. All these advantages facilitate the integration of graphitic carbon into existing conventional semiconductor devices. Based on the

aforementioned reasons, the FCVA graphitic carbon thin film is a strong candidate for a cost-effective p-type Si Schottky diode.

Sentaurus TCAD simulation software has been used to model the fabricated C/p-Si Schottky diodes in 2-D and 3-D. The experimental *I-V* characteristics suggested the presence of an interfacial resistive layer between the graphitic carbon and Si and this was accounted for in the M-R-S TCAD diode structure model. The Barrier lowering model was activated in TCAD to include image force effects reported in literature and provide better agreement with measurements. Adjusting the interface resistance (R_D) and 'metal' work function ($q\phi_m$) of the modelled graphitic contact has led to achieving an excellent agreement between the experimental and simulated *I-V* characteristics. For the M-R-S model, the agreement between the experimental and simulated *I-V* results in the reverse *I-V* region has improved significantly compared to simulation using the M-I-S model. The optimum values for the best fits are presented and their reliability in interpretation is discussed. A high degree of confidence can be had in the value of work function determined for the FCVA deposited graphitic carbon electrode using the M-R-S technique. The work function determined by this method fell within the range commonly reported for carbon films with a high graphitic fraction. It cannot be reliably measured experimentally. The modelling thus provides additional insight and suggests methods for improving device performance. In conclusion, M-R-S TCAD simulations are reliable for projecting the performance of graphitic carbon Schottky diodes and hence can be used as "pathway indicators" in future optimisations.

6.2 Future work

The investigated graphitic carbon/p-Si Schottky diodes have a very simple structure. There is an area for improving the performance of the devices by fabricating a more optimised structure that includes:

1) Guard rings to avoid leakage currents flowing outside the active interface of the device.

2) SiO_2 passivation layer to protect the device and reduce the possibility of contamination.

3) Reducing the series resistance of the device by optimising the geometry.

The M-R-S simulations have predicted a significant increase in the RR of the C/p-Si Schottky diodes when the work function of the graphitic carbon thin films was reduced. From a practical point of view, lowering the value of work function can be achieved by introducing dopants during carbon depositions.

The work presented in this thesis can be extended to several directions:

- Investigating the effect of doping type of silicon by fabricating graphitic carbon Schottky diodes on n-type Si substrates and optimise the FCVA deposition conditions (i.e. substrate bias and substrate temperature) accordingly. A thorough investigation of Si substrate properties (e.g. orientation (111 or 100), doping

concentration, growth (CZ or FZ), surface roughness and defect level) would also aid in future optimisations.

- For carbon thin films deposited using FCVA, additional XTEM results are required in order to comprehensively analyse the interfacial layer and improve the TCAD models.

- Investigating the effect of diode size on the value of the ideality factor (*n*).

- Power diode applications.

Appendix A

Description of the Metal-Resistor-Semiconductor (M-R-S) TCAD modelling in Sentaurus WorkBench (SWB) environment

In this appendix, a brief description highlighting the process of constructing the 2-D and 3-D M-R-S models in Sentaurus TCAD is presented. As stated in section 2.3, SWB is the tool responsible for managing all operations in this TCAD 'Project' which was constructed to numerically model the fabricated samples. Figure A.1 shows a screenshot displaying the 'simulation tree' in SWB tool with a single simulation 'Experiment 1'. It also shows the tool flow (i.e. SDE followed by SDEVICE) and a set of variables (metal, wp, wm, and p_doping for SDE and WF, Rd, V_start, and V_stop for SDEVICE) that were customised to allow for direct variation within the project in SWB. Simulation experiments are very useful for performing long iterative simulations with multiple parameter variation. An example of a TCAD project with 40 experiments is shown in Figure A.2.

For the M-R-S diode structure generation, an input file with the name *sde_dvs.cmd* must be written and included as a command file for SDE in order to generate the output files necessary for SDEVICE to run the numerical modelling/simulation. Among SDE output files, the file ending with the *_msh.tdr* contains the discretised structure (MESH) of the device which is used by SDEVICE to discretise the system equations. In addition to SDE output files, SDEVICE requires three input files; a command file named *sdevice_des.cmd* where the numerical device physics and boundary conditions are defined, *datexcodes.txt* and *sdevice.par* files to create new materials in the library database (i.e. assigning a name, type, and colour) and to define material's numerical parameters, respectively.

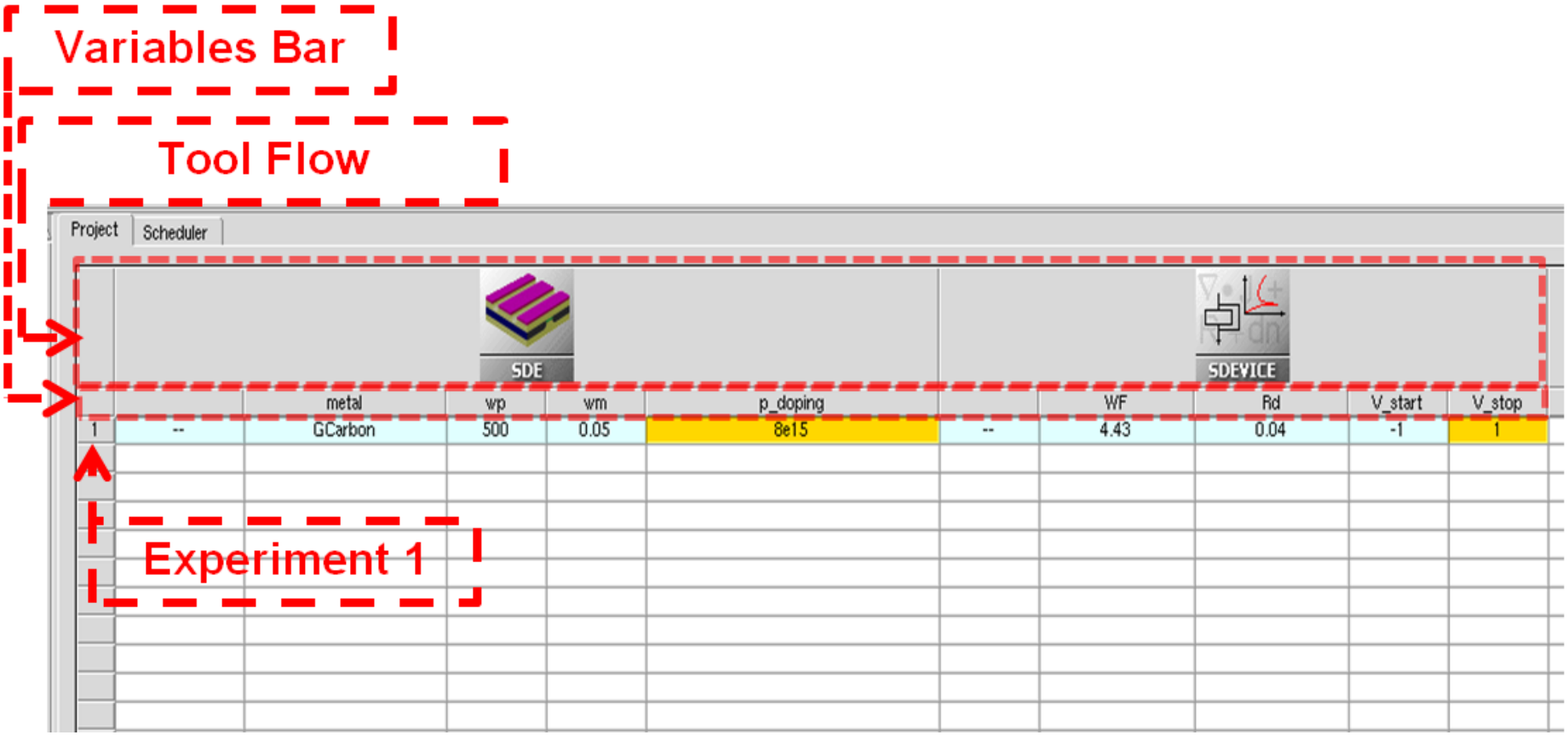

Figure A.1: Screenshot of the TCAD project constructed for M-R-S modelling within Sentaurus Workbench (SWB) environment in TCAD. In the Variables Bar, there are: metal which defines the material used as Schottky metal, wp is the thickness of p-Si [μm], wm is the thickness of the metal [μm], p_doping is the Boron doping concentration [cm^{-3}], WF is the effective metal work function [eV], Rd is the distributed contact resistance [$\Omega\ cm^2$], V_start and V_stop are bias ramping goals [V] defining the range of bias voltage in the *I-V* plot.

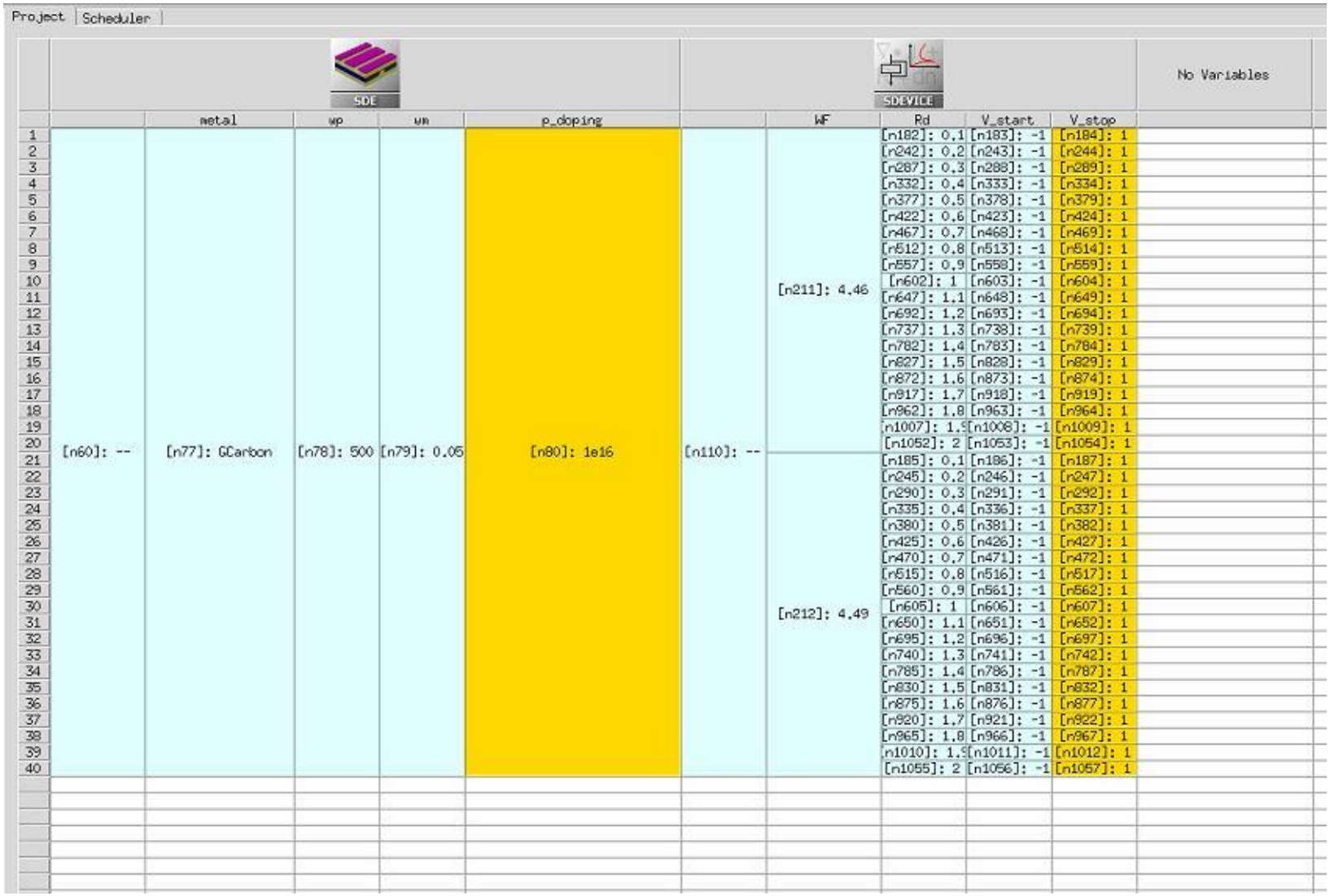

Figure A.2: Screenshot of a TCAD project showing 40 experiments. The targeted parameters for iteration are WF (simulated at 4.46 eV and 4.49 eV) and Rd (simulated in the range 0.1 – 2 in steps of 0.1 Ω cm^2).

Once SDEVICE successfully completes the simulation, it generates two types of output files that contain the required results from the simulation. The first output file ending with *_des.tdr* contains data about the distribution of internal quantities within the modelled structure (e.g. electrostatic potential, current density, and electric field) that can be visualised in either 2D/3D output maps or plotting the quantity with respect to x,y or z after 'cutting' the structure in a specific point. The second output file ending with *_des.plt* contains data about electrical characteristics (i.e. this is the file that shows the *I-V* plot for the simulated structure).

Appendix B

SDE and SDEVICE command files for 2D and 3D M-R-S diode structures

```
; *********************************************************************
; *****COMMAND FILE (CODE) FOR GENERATION OF THE 2D M-R-S DIODE*****
;  **********STRUCTURE IN SDE- sde_dvs.cmd**********
; *********************************************************************

; ********** INITIALIZATION **********
; clear structure
(sde:clear)
; New-replace-old option (default)
(sdegeo:set-default-boolean "ABA")
; ********** DEFINITIONS **********
; define lengths (x-direction), Lp is the length of p-Si region and Lm is the length of metal
;electrode region
(define Lp 1255)
(define Lm 355)
; define metal electrode region thickness (y-direction), any variable between @ is defined in
;SWB tree
(define wm @wm@)
; define p-Si region thickness (y-direction)
(define wp @wp@)
; Doping Parameter
```

```
(define p_doping @p_doping@)
; Metal Type
(define metal "@metal@")
; MESH Parameters
(define xmax 100)
(define xmin 0.01)
(define ymax 100)
(define ymin 0.01)

; ****************************** GEOMETRY ********************************
; Convention: x=length y=thickness
; create metal
(sdegeo:create-rectangle (position 450 0 0) (position (+ 450 Lm) wm 0) metal "metal")
; create p-Si region
(sdegeo:create-rectangle (position 0 wm 0) (position Lp (+ wm wp) 0) "Silicon"
"Semiconductor")

; ****************************** CONTACTS ********************************
; a) Set Vertices
; 1st vertex on m_contact
(sdegeo:insert-vertex (position 450 0 0))
; 2nd vertex on m_contact
(sdegeo:insert-vertex (position (+ 450 Lm) 0 0))
; 1st vertex on p_contact
(sdegeo:insert-vertex (position 0 (+ wm wp) 0))
```

```
; 2nd vertex on p_contact
(sdegeo:insert-vertex (position Lp (+ wm wp) 0))
; b) Set Edges
;m_contact
(sdegeo:define-contact-set "m_contact" 4 (color:rgb 1 0 0) "##")
(sdegeo:set-current-contact-set "m_contact")
(sdegeo:define-2d-contact (find-edge-id (position (* Lp 0.5) 0 0)) "m_contact")
;p_contact
(sdegeo:define-contact-set "p_contact" 4 (color:rgb 1 0 0) "##")
(sdegeo:set-current-contact-set "p_contact")
(sdegeo:define-2d-contact (find-edge-id (position (* Lp 0.5) (+ wm wp) 0)) "p_contact")

; ********************************** DOPING **********************************
; p-region
(sdedr:define-constant-profile "p-doping-profile" "BoronActiveConcentration"
@p_doping@)
(sdedr:define-constant-profile-region "p-doping-placement" "p-doping-profile"
"Semiconductor")
(sdedr:define-constant-profile-placement "p-doping placement" "p-doping-profile" "p-
doping-window")

; ********************************** MESH **********************************
; Whole Domain
(sdedr:define-refeval-window "domain-ref" "Rectangle" (position 0 0 0) (position Lp (+ wm
wp) 0))
```

```
(sedr:define-refinement-size "domain-ref-size" xmax ymax xmin ymin)
(sedr:define-refinement-placement "domain-ref-pl" "domain-ref-size" "domain-ref")
; MS Junction Refinement
(sedr:define-refeval-window "junction-ref" "Rectangle" (position 450 (- wm 0.01) 0)
(position (+ 450 Lm) (+ wm 0.5) 0))
(sedr:define-refinement-size "junction-ref-size" (/ xmax 100) (/ ymax 100) (/ xmin 40) (/
ymin 40))
(sedr:define-refinement-placement "junction-ref-pl" "junction-ref-size" "junction-ref")
; Building MESH
(sde:build-mesh "snmesh" "-a -c boxmethod" "n@node@")
; ********** END **********
```

```
; ********************************************************************************
; *****COMMAND FILE (CODE) FOR GENERATION OF THE 3D M-R-S DIODE*****
;  **********************STRUCTURE IN SDE- sde_dvs.cmd************************
; ********************************************************************************

; ****************************** INITIALIZATION ******************************
; clear structure
(sde:clear)
; New-replace-old option (default)
(sdegeo:set-default-boolean "ABA")

; ******************************** DEFINITIONS *******************************
; define lengths (x-direction), Lp is the length of p-Si region and Lm is the length of metal
(define Lp 667.5)
; define metal electrode region thickness (y-direction),
(define wm @wm@)
; define p-Si region thickness (y-direction),
(define wp @wp@)
; Doping Parameter
(define p_doping @p_doping@)
; Metal Type
(define metal "@metal@")
; MESH Parameters
(define xmax 100)
(define xmin 0.01)
```

```
(define ymax 100)
(define ymin 0.01)
(define zmax 100)
(define zmin 0.01)

; ******************************* GEOMETRY *********************************
; Convention: x and y=length z=thickness
; create p region
(sdegeo:create-cuboid (position 0 0 0)  (position Lp Lp wp) "Silicon" "Semiconductor" )
; create metal
(sdegeo:create-cylinder (position (* Lp 0.5) (* Lp 0.5) wp)  (position (* Lp 0.5) (* Lp 0.5) (+
wp wm))  200 metal "metal" )

; ******************************* CONTACTS *********************************
;p_contact
(sdegeo:define-contact-set "p_contact" 4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-3d-contact (list (car (find-face-id (position (* Lp 0.5) (* Lp 0.5) 0))))
"p_contact")
(sdegeo:set-current-contact-set "p_contact")
;m_contact
(sdegeo:define-contact-set "m_contact" 4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-3d-contact (list (car (find-face-id (position (* Lp 0.5) (* Lp 0.5) (+ wp
wm))))) "m_contact")
(sdegeo:set-current-contact-set "m_contact")
```

```
; ********************************* DOPING *********************************
; p-region
(sdedr:define-constant-profile "p-doping-profile" "BoronActiveConcentration"
@p_doping@)
(sdedr:define-constant-profile-region "p-doping-placement" "p-doping-profile"
"Semiconductor")
(sdedr:define-constant-profile-placement "p-doping placement" "p-doping-profile" "p-
doping-window")

; ********************************* Trimming *********************************
(sdegeo:chop-domain (list 0 0  (* Lp 0.5) 0   (* Lp 0.5) (* Lp 0.5)))

; ********************************* MESH *********************************
; Whole Domain
(sdedr:define-refeval-window "domain-ref" "cuboid" (position 0 0 0) (position (* Lp 0.5) (*
Lp 0.5) (+ wm wp)))
(sdedr:define-refinement-size "domain-ref-size" xmax ymax zmax xmin ymin zmin)
(sdedr:define-refinement-placement "domain-ref-pl" "domain-ref-size" "domain-ref")
; MS Junction Refinement
(sdedr:define-refeval-window "junction-ref" "cuboid" (position 123.75 123.75 (- wp 0.5))
(position (* Lp 0.5) (* Lp 0.5) (+ wp 0.1)))
(sdedr:define-refinement-size "junction-ref-size" (/ xmax 100) (/ ymax 100) (/ zmax 100) (/
xmin 40) (/ ymin 40) (/ zmin 40))
(sdedr:define-refinement-placement "junction-ref-pl" "junction-ref-size" "junction-ref")
```

```
; BUILDING MESH
(sde:build-mesh "snmesh" "-a -c boxmethod" "n@node@")
********************************** END **********************************

*****************************************************************************
***MATERIAL PARAMETR FILE FOR GRAPHITIC CARBON (GCarbon) FOR THE***
********* 2D and 3D M-R-S TCAD MODELLING IN SDEVICE – sdevice.par *********
*****************************************************************************

Material = "GCarbon" {

Bandgap
{ * For conductors Band Gap is zero and the following parameters are used:
        WorkFunction = 4.43  # [eV]
  * for backward compatibility Chi0 could be used to define the work function.
}

Resistivity
{ * Resist(T) = Resist0 * ( 1 + TempCoef * ( T - 273 ) )
        Resist0= 2.4500e-06   # [ohm*cm]
        TempCoef       = -0.5000e-03 # [1/K]
}
}
********************************** END **********************************
```

```
**************************************************************************
** COMMAND FILE (CODE) FOR MODELLING OF THE 2D and 3D M-R-S DIODE **
********** STRUCTURES IN SDEVICE- sdevice_des.cmd ******************
**************************************************************************

File
{
**** INPUT FILES
* geometry, contacts, doping and mesh
Grid ="@tdr@"
* physical parameters
Parameter ="@parameter@"
**** OUTPUT FILES
* to visualize disributed variables
Plot = "n@node@_des.tdr"
* to visualize electrical characteristics at the electrodes
Current= "n@node@_des.plt"
}
Electrode
{
* defines which contacts have to be treated as electrodes
* & initial boundary conditions
* obviously, electrode names must match the contact names of the
* sde_dvs.cmd file
{ name="p_contact" voltage=0.0}
{ name="m_contact" voltage=0.0}
```

```
}
Physics (Material= "GCarbon")
{
MetalWorkfunction (workfunction=@WF@)
}
Physics
{
Mobility (
DopingDependence
HighFieldSaturation
)
Fermi

EffectiveIntrinsicDensity ( oldSlotboom )
Temperature= 300
AreaFactor = 355  *For 3-D structure, AreaFactor =8
}

Physics(RegionInterface = "metal/Semiconductor")
{
Schottky DistResist= @Rd@
Schottky BarrierLowering
}
Plot
{
```

```
* On-mesh-defined variables to be saved in the .tdr output file
*- Doping Profiles
Doping DonorConcentration AcceptorConcentration
*- charge, field, potentail and potential energy
SpaceCharge
ElectricField/Vector Potential
BandGap EffectiveBandGap BandGapNarrowing ElectronAffinity
CondutionBandEnergy ValenceBandEnergy
*- Carrier Denisities:
EffectiveIntrinsicDensity IntrinsicDensity
eDensity hDensity
eQuasiFermiEnergy hQuasiFermiEnergy
*- Currents and current components:
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eMobility hMobility eVelocity hVelocity
Current/Vector eCurrent/Vector hCurrent/Vector
eDriftVelocity/Vector hDriftVelocity/Vector
*- SRH & interfacial traps
SRHrecombination
tSRHrecombination
*- Band2Band Tunneling & II
eBand2BandGeneration hBand2BandGeneration Band2BandGeneration
eAvalanche hAvalanche Avalanche
}
Math
```

```
{
Number_Of_Threads = maximum
* use previous two solutions (if any) to extrapolate next
Extrapolate
* use full derivatives in Newton method
Derivatives
* control on relative and absolute errors
-RelErrControl
* relative error= 10^(-Digits)
Digits=10
* numerical parameter for space-charge regions
eDrForceRefDens=1e10
hDrForceRefDens=1e10
* maximum number of iteration at each step
Iterations=20
* choosing the solver of the linear system
Method=ParDiSo
* display simulation time in 'human' units
Wallclock
* display max.error information
CNormPrint
* to avoid convergence problem when simulating defect-assisted tunneling
NoSRHperPotential
}
Solve
```

```
{
*EQUILIBRIUM
coupled {poisson}
* TURN-ON
* decreasing p_contact to goal
quasistationary (InitialStep = 0.0010 MaxStep = 0.0010 MinStep= 0.0000001
Goal {name= "p_contact" voltage = @V_start@}
plot { range=(0, 1) intervals=1 }
)
{coupled {Poisson Electron Hole} }
*raising p_contact to goal
quasistationary (InitialStep = 0.0010 MaxStep = 0.0010 MinStep = 0.0000001
Goal {name= "p_contact" voltage = 0}
)
{coupled {Poisson Electron Hole} }
quasistationary (InitialStep = 0.0010 MaxStep = 0.0010 MinStep = 0.0000001
Goal {name= "p_contact" voltage = @V_stop@}
plot { range=(0, 1) intervals=1 }
)
{coupled {Poisson Electron Hole} }
```

Appendix C

Convergence and error handling in M-R-S modelling in Sentaurus TCAD

Meshing is one of the most critical parts in building an accurate TCAD model. Defining an efficient numerical mesh in which convergence can be achieved at reasonable simulation time is a challenging task. Convergence here refers to the invariance of the *I-V* characteristics with respect to variations of the mesh. In other words, the element dimensions in the mesh are gradually reduced until the change in the *I-V* results from one mesh size to the next is negligible. Figures C1 and C2 presents a case where the element mesh density across and near the MS interface in the M-R-S diode structure was varied and its effect on the *I-V* plot, respectively. The mesh in part (a) of figure C1 has an average of ~ 600 total mesh elements while part (b) mesh has ~ 5000 (fit).

Numerical simulator (SDEVICE) applies a scheme, developed by Bank and Rose [60], to find the solution. The scheme solves the nonlinear system by Newton's method. In order to determine the value of an equation variable x, the Newton iteration keeps updating such that the computed update Δx (after n^{th} iteration) is small enough. The iteration stops (converges) if the following inequality is fulfilled:

$$\frac{\left|\frac{\Delta x}{x^*}\right|}{\varepsilon_R \left|\frac{x}{x^*}\right| + \varepsilon_A} < 1$$

The parameter $\varepsilon_R = 10^{-Digits}$ is the relative error criterion and its value is set by specifying a value for the keyword 'Digits' in the simulator.

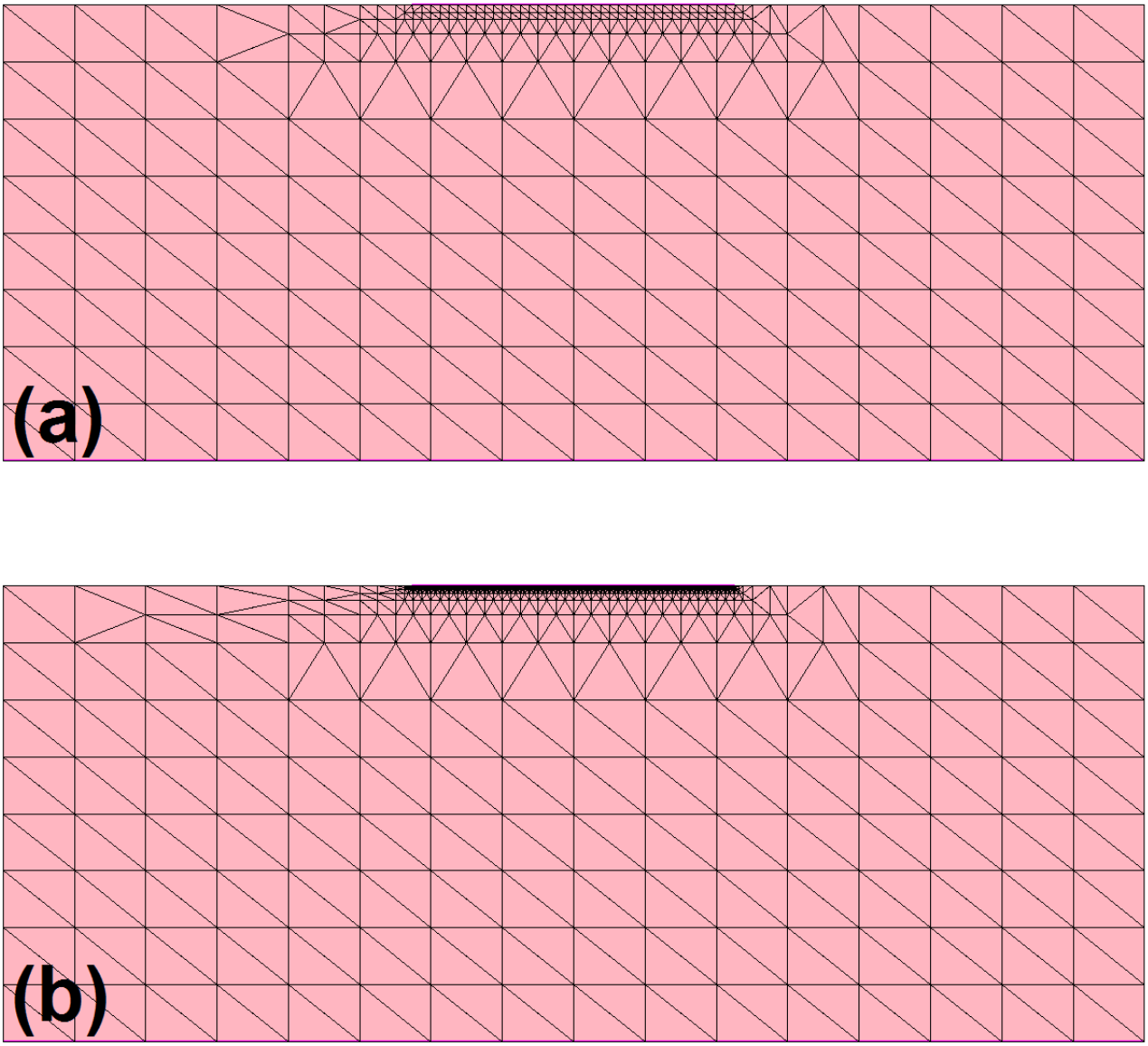

Figure C.1: (a) 2-D M-R-S diode structure showing coarse meshing near and around the MS interface. (b) the best fit mesh for the 2-D M-R-S diode structure.

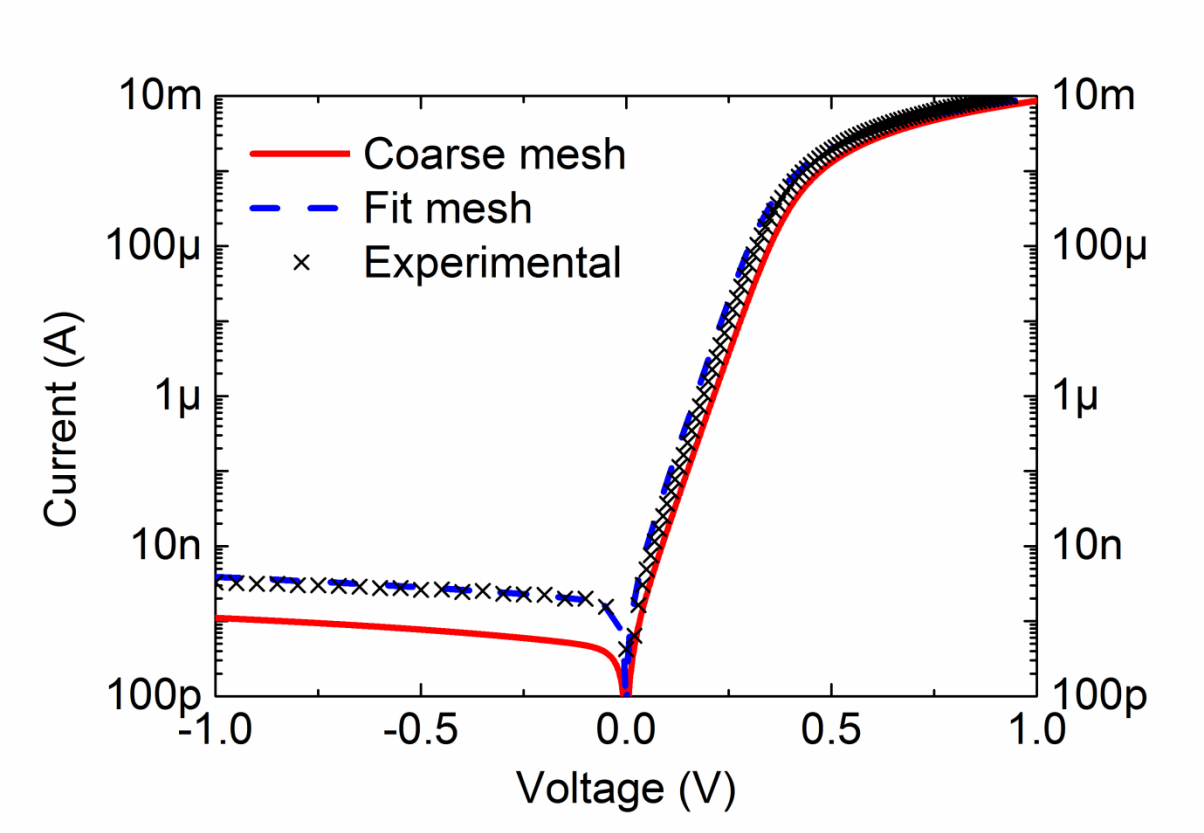

Figure C.2: Current-Voltage plots for the 2-D M-R-S diode structure generated in Sentaurus TCAD showing the effect of mesh density.

For our work, the specified value for Digits is 10. The parameter ε_A is the absolute error criterion and its value is defined for each equation ($\varepsilon_A = 1\text{x}10^{-5}$ for electron and hole continuity equations and $\varepsilon_A = 1\text{x}10^{-3}$ for Poisson equation). The parameter x^* is the normalization factor ($x^* = 1.48\text{x}10^{10}$ cm^{-3}, which is the intrinsic carrier density, for electron and hole continuity equations and $x^* = 25.8$ mV, which is the thermal voltage, for Poisson equation). The inequality can be simplified into two limiting cases as follows:

For large values of x ($|x| \rightarrow \infty$)

$$\left|\frac{\Delta x}{x}\right| < \varepsilon_R \qquad \text{(relative error criterion)}$$

For small values of x ($|x| \to 0$)

$$\left|\frac{\Delta x}{x^*}\right| < \varepsilon_A \qquad \text{(absolute error criterion)}$$

References

[1] K. F. Braun, "Über die Stromleitung durch Schwefelmetalle," *Ann. Phys. Chem.*, vol. 229, pp. 556-563, 1874.

[2] G. W. Pickard, "Means for Receiving Intelligence Communicated By Electric Waves," U. S. Patent 836,531 (Filed August 20, 1906).

[3] L. Łukasiak *et al*., "History of Semiconductors," *J. Telecomun. Inf. Technol.*, vol. 1, pp. 3-9, 2010.

[4] W. Schottky, "Halbleitertheorie der Sperrschicht," *Naturwissenschaften,* vol. 26, pp. 843-843, 1938.

[5] N. F. Mott, "Note on the contact between a metal and an insulator or semi-conductor," *Math. Proc. Cambridge Philos. Soc.*, vol. 34, pp. 568-572, 1938.

[6] S. M. Sze *et al*., *Physics of semiconductor Devices*, 3rd ed., John Wiley & Sons, New Jersy, 2006.

[7] T. Rinken, *Biosensors - Micro and Nanoscale Applications*, InTech, Croatia, 2015. DOI: 10.5772/60510. Available from: http://www.intechopen.com/books/biosensors-micro-and-nanoscale-applications/new-materials-for-the-construction-of-electrochemical-biosensors

[8] K.S. Novoselov *et al*., "Electric field effect in atomically thin carbon films," *Science* vol. 306, pp. 666–669, 2004.

[9] C. C. Chen *et al*., "Graphene-silicon Schottky diodes," *Nano Lett.*, vol. 11, pp. 1863-1867, 2011.

[10] M. Mohammed *et al*., "Junction investigation of graphene/silicon Schottky diodes," *Nanoscale Res. Lett*., vol. 7, pp. 302, 2012.

[11] D. P. Sinha *et al*., "Ideal Graphene/Silicon Schottky Junction Diodes," *Nano Lett.*, vol. 14, pp. 4660-4664, 2014.

[12] S. Tongay *et al*., "Graphite based Schottky diodes formed on Si, GaAs, and 4H-SiC substrates," *Appl. Phys. Lett.*, vol. 95, pp. 222103, 2009.

[13] S. M. Sultan *et al.*, "Electrical behavior of nanocrystalline graphite/p-Si Schottky diode," *in IEEE 16th Int. conf. Nanotechnol. (IEEE-NANO*), pp. 307-310, 2016.

[14] D. W. M. Lau *et al*., "Abrupt Stress Induced Transformation in Amorphous Carbon Films with a Highly Conductive Transition Phase," *Phys. Rev. Lett*., vol. 100, pp. 176101, April 2008.

[15] D. W. M. Lau *et al*., "The structural phases of non-crystalline carbon prepared by physical vapour deposition," *Carbon*, vol. 47, pp. 3263-3270, 2009.

[16] D. W. M. Lau *et al*., "Microstructural investigation supporting an abrupt stress induced transformation in amorphous carbon films," *J. Appl. Phys*., vol. 105, pp. 084302, 2009.

[17] R. Minixhofer *et al*., "TCAD as an integral part of the semiconductor manufacturing environment," *in SISPAD Proc.*, pp. 9-16, 2006 (invited).

[18] International Technology Roadmap for Semiconductors (2004 Edition).

[19] R. D. Thompson *et al*., "Schottky barrier of nonuniform contacts to n-type and p-type silicon," *J. Appl. Phys.*, vol. 53, pp. 4285–4288, 1982.

[20] Jurgan H. Werner *et al*., "Barrier inhomogeneities at Schottky contacts," *J. Appl. Phys.*, vol. 69, pp. 1522–1533, 1991.

[21] H. Cetin *et al*., "Temperature dependence of electrical parameters of the Au/n-InP Schottky barrier diodes," *Semicond. Sci. Technol.*, vol. 20, pp. 625, 2005.

[22] S. M. Goodnick *et al*., "Computational electronics," *in Encyclopedia of Materials: Science and Technology*, vol. 2, pp. 1456–1471, Elsevier, New York, 2001.

[23] D. Vasileska *et al*.,"Computational electronics," *Mater. Sci. Eng. R-Rep*., vol.38, pp. 181–236, 2002.

[24] See https://www.synopsys.com/silicon/tcad.html for details.

[25] Synopsys® Sentaurus Device User Guide (2015).

[26] X. Li *et al.*, "The graphene-semiconductor Schottky junction," *Phys. Today*, vol. 69, pp. 46-51, 2016.

[27] G. K. Bhagavat *et al.*, "Semiconducting amorphous carbon films and carbon-single-crystal silicon heterojunctions," *Thin Solid Films*, vol. 64, pp. 57-62, 1979.

[28] D. E. Bradley, "Evaporated carbon films for use in electron microscopy," *Br. J. Appl. Phys.*, vol. 5, pp. 65-66, 1953.

[29] G. Amaratunga *et al.*, "Heterojunction diodes formed using thin-film C containing polycrystalline diamond and Si," *IEEE Electron Device Lett.*, vol. 11, pp. 33-35, 1990.

[30] G. A. J. Amaratunga *et al.*, "Crystalline diamond growth in thin films deposited from a CH_4/Ar rf plasma," *Appl. Phys. Lett.*, vol. 55, pp. 634-635, 1989.

[31] G. A. J. Amaratunga *et al.*, "Amorphous diamond-Si semiconductor heterojunctions," *Appl. Phys. Lett.*, vol. 59, pp. 69-71, 1991.

[32] V. S. Veerasamy *et al*., "Optical and electronic properties of amorphous diamond," *Diamond Re1. Mater*., vol. 2, pp. 782-787, 1993.

[33] V. S. Veerasamy *et al*., "n-type doping of highly tetrahedral diamond-like amorphous carbon," *J. Phys. Cond. Mater*., vol. 5, pp. L169, 1993.

[34] V. S. Veerasamy *et al*., "Nitrogen doping of highly tetrahedral amorphous carbon," *Phys. Rev, B*, vol. 48, pp. 17954, 1994.

[35] V. S. Veerasamy *et al.*, "Properties of n-type tetrahedral amorphous carbon (ta-C)/p-type crystalline silicon heterojunction diodes," *IEEE Trans. Electron Devices*, vol. 42, pp. 577-585, 1995.

[36] H. A. Yu *et al.*, "Photovoltaic cell of carbonaceous film/n-type silicon," *Appl. Phys. Lett.*, vol. 68, pp. 547-549, 1996.

[37] H. A. Yu *et al.*, "The junction characteristics of carbonaceous film/n-type silicon (C/n-Si) layer photovoltaic cell," *Appl. Phys. Lett*., vol. 69, pp. 3042-3044, 1996.

[38] M. Chhowalla *et al*., "Influence of ion energy and substrate temperature on the optical and electronic properties of tetrahedral amorphous carbon (ta-C) films," *J. Appl. Phys*., vol. 81, pp. 139-145, 1997.

[39] N. Konofaos *et al*., "Device characterization for amorphous diamond-like carbon–silicon heterojunctions," *J. Appl. Phys*., vol. 84, pp. 4634-4636, 1998.

[40] X. Gao *et al*., "Effect of gas pressure on current-voltage characteristics of amorphous carbon film/silicon heterojunction," *Appl. Phys. Lett*., vol. 91, pp. 092104, 2007.

[41] S.-S. Yap *et al*., "Investigation of diamond-like carbon/silicon heterojunctions deposited by pulsed Nd:YAG laser," *Vacuum*, vol. 82, pp. 1449-1451, 2008.

[42] R. K. Gupta *et al*., "Current–voltage characteristics of p-Si/carbon junctions fabricated by pulsed laser deposition," *Microelectron. Eng*., vol. 87, pp. 221-224, 2010.

[43] X. Li *et al*., "Graphene-On-Silicon Schottky Junction Solar Cells," *Adv. Mater*., vol. 22, pp. 2743-2748, 2010.

[44] C. Yim *et al*., "Carbon–Silicon Schottky Barrier Diodes," *Small*, vol. 8, pp. 1360-1364, 2012.

[45] C. Yim *et al*., "Investigation of carbon–silicon Schottky barrier diodes," *phys. Status solidi B*, vol. 249, pp. 2553-2557, 2012.

[46] M. Stelzer *et al*., "Graphenic Carbon-Silicon Contacts for Reliability Improvement of Metal-Silicon Junctions," *in IEDM Proc.*, 2016.

[47] X. Li *et al.*, "Carbon/Silicon Heterojunction Solar Cells: State of the Art and Prospects," *Adv. Mater.*, vol. 27, pp. 6549-6574, 2015.

[48] A. Di Bartolomeo, "Graphene Schottky diodes: An experimental review of the rectifying graphene/semiconductor heterojunction," *Phys. Rep*., vol. 606, pp. 1-58, 2016.

[49] Chin Scott, SAS JPG Filtered cathodic vacuum arc deposition system, Online Image, SET, Melbourne, Vic, accessed 23 May, 2017, Available from: http://mams.rmit.edu.au/s3am7fxhra1x.jpg

[50] M. Kracica *et al*., "Ohmic and rectifying contacts to n-SiC formed by energetic deposition of carbon," *in MRS Online Proc*., vol. 1693, pp. 1-6, 2014.

[51] G. Masetti *et al.*, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Trans. Electron Devices*, vol. 30, pp. 764-769, 1983.

[52] C. Canali *et al*., "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Trans. Electron Devices*, vol. 22, pp. 1045-1047, 1975.

[53] M. Pinto. *Comprehensive semiconductor device simulation for silicon ULSI*. Ph.D. Dissertation: Stanford University, 1990.

[54] A. Di Bartolomeo *et al.*, "Tunable Schottky barrier and high responsivity in graphene/Si-nanotip optoelectronic device," *2D Mater*., vol. 4, pp. 1-11, 2016.

[55] X. Zhang *et al*., "Doping enhanced barrier lowering in graphene-silicon junctions," *Appl. Phys. Lett.*, vol. 108, pp. 263502, 2016.

[56] S. J. Sque *et al*., "The transfer doping of graphite and graphene," *Phys. Status Solidi A*, vol. 204, pp. 3078-3084, 2007.

[57] N. Ooi *et al*., "Density functional study of graphite bulk and surface properties," *Carbon*, vol. 44, pp. 231-242, 2006.

[58] M. Kracica *et al.*, "Rectifying electrical contacts to n-type 6H─SiC formed from energetically deposited carbon," *Carbon*, vol. 102, pp. 141-144, 2016.

[59] J. Ropertson, "Diamond-like amorphous carbon," *Mater. Sci. Eng., R*, vol. 37, pp. 129-281, 2002.

[60] R. E. Bank *et al*., "Global approximate Newton methods," *Numerische Mathematik*, vol. 37, pp. 279-295, 1981.